Embedded PHY parameters for MPCP

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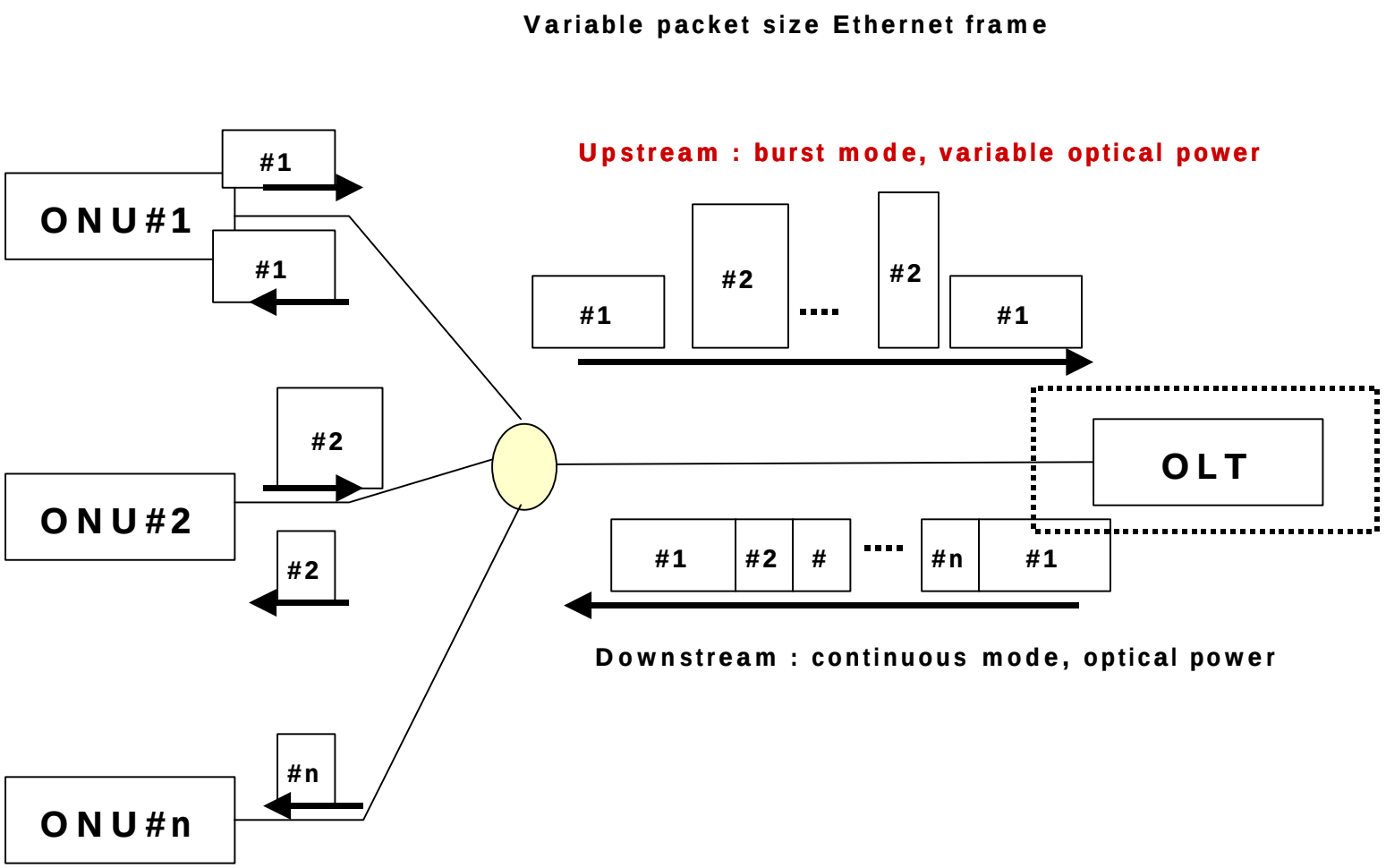
IEEE802.3ah, Edinburgh, May,2002

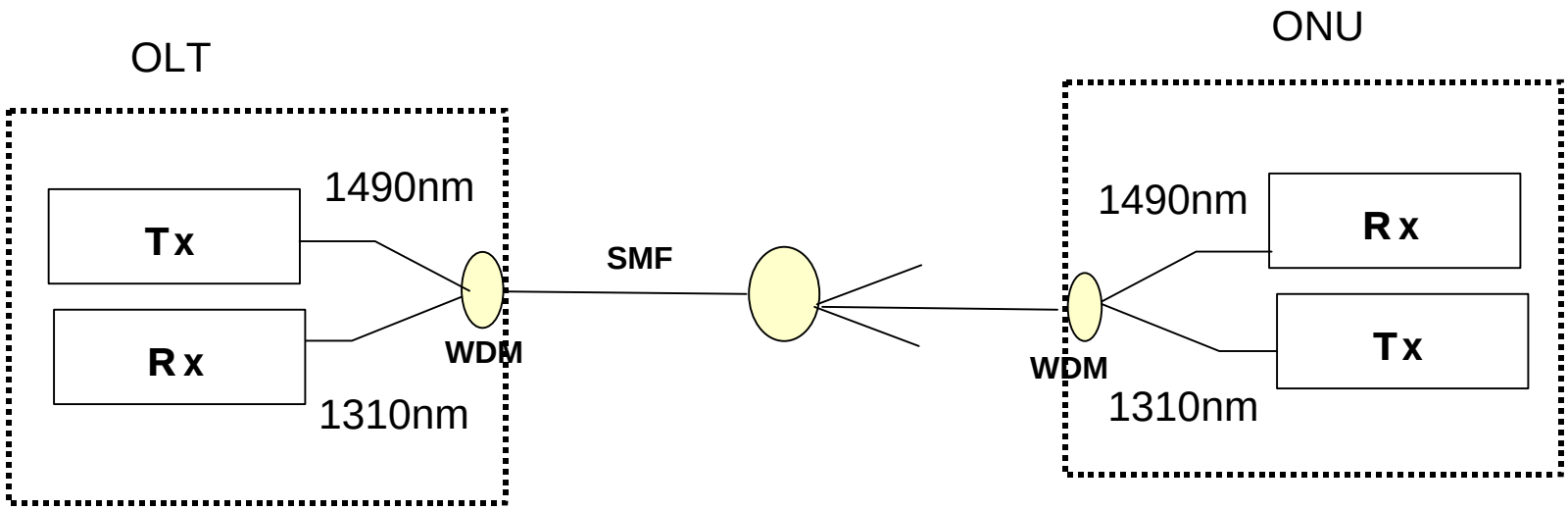
EPON architecture



What to consider ….

- MPCP is to be addressed in consideration of available PMD parameters for EPON, as higher layer can adapt to PHY capacity
- Conventional IFG= 96 bits is valid for CSMA/CD, not for EPON using TDM
- Timing model, scheduling cycle, and MPCP parameters including guard time are coupled with PHY parameters , which affect system performance
- Burst mode operation has sensitivity 2dB worse and worse jitter condition than continuous mode operation
- APON based on cell transmission has relatively tight timing spec. while EPON based on packet transmission has less tight spec.

EPON modules for uplink



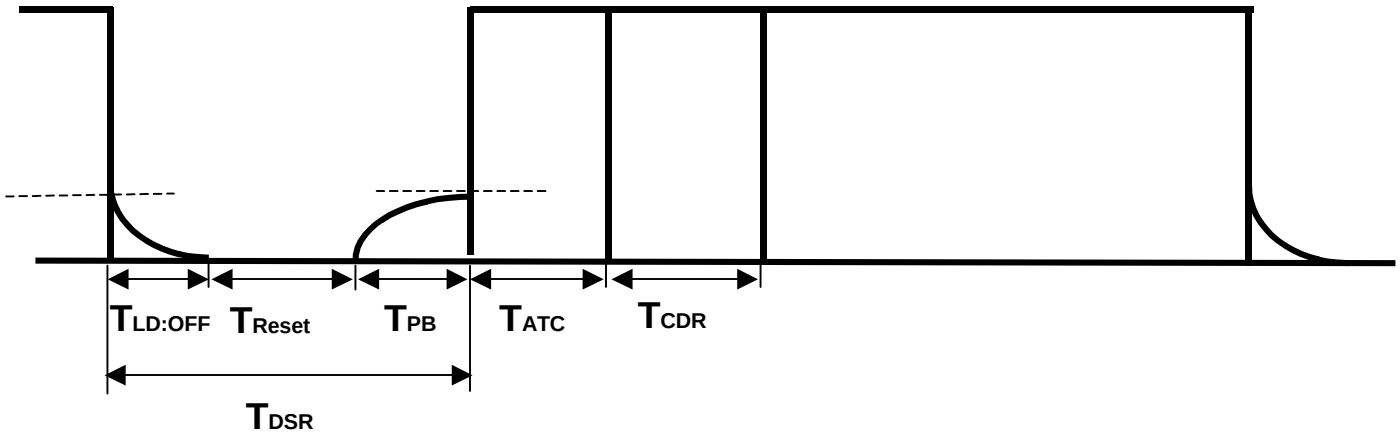
BM TIA with dynamic range >25dB

BM Postamp

CDR

BM Laser Driver

Parameter Definition



- $T_{LD:OFF}$: **LD turn off time**
- T_{PB} **: LD prebias time**
- T_{ATC} **: threshold-level recovery time**
- T_{CDR} **: clock recovery time**
- T_{Reset} **: reset time**
- T_{DSR} **: dynamic sensitivity recovery time**

1.25Gbps Transceiver parameters

			BM Transc. 2R	GE Transc.
		Symbol (unit)	2R	CM 2.5Gbps w/ sw
ONU Tx	Rise/fall time (20-80%)	(ns)	<0.3	<0.3
	LD prebias time	T_{PB} (ns)	2 - 12.8	>10
	LD turn off time	$T_{LD:OFF}$ (bit)	1 - 2	>10
	ER	dB	>10	>10
OLT Rx	Threshold-level recovery time	T_{ATC} (bit)	16	
	Clock recovery time	T_{CDR} (bit)	NA	
	Dyn. sensitivity recovery time	T_{DSR} (bit)	>20 - 24	

Implementation

- **Bit synch.**

  (i) With 2R Rx + legacy Ethernet SERDES chip

  - CDR with current Ethernet chip take 160-200bits (including comma synch.)

  - no change of PHY interface, compatible with existing Ethernet PHY chip

  - need longer guard band

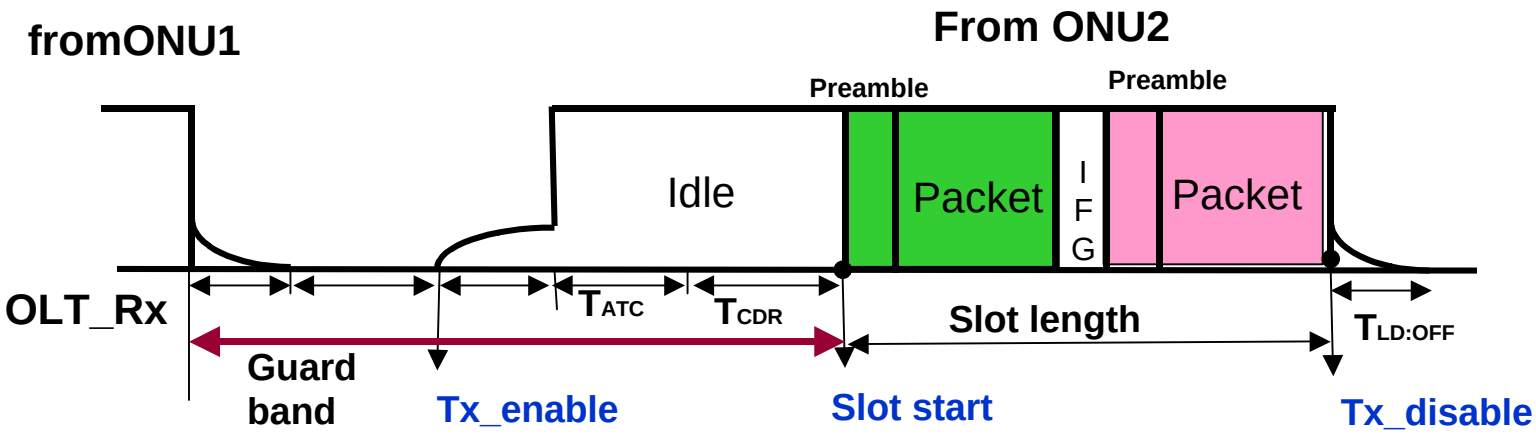
  (ii) With 3R Rx + Ethernet SERDES chip with optional clock interface change

  - need shorter guard band

- **PHY layer Overhead is estimated 3-6 bytes by most of FSAN companies (2002, March, EFM PMD track)**

- **Adapting to OLT, and universal spec for ONUs would be desirable (centralized system)**

Signaling by MAC



Most of BM Rx have DSR time longer than (LD:ON + LD:OFF) time

Guard band = T_{DSR} + T_{ATC}+T_{CDR}+ Td

Td is guard band for clock drift due to clock mismatch, RTT change, clock resolution and variable delay

Open issue: Size of IFG ? From 96 bits down to 0 bit

Guard band Model

- **Fixed GB**
  - **enough guard band to cover available PMD device capabilities**

- **Configurable GB**
  - **depends on consisting PMD device capabilities**
  - **OLT determines GB as a total of its DSR, ATC, CDR time plus extra guard time for clock drift**

  (if (LD:ON +LD:OFF) time> DSR time, replace DSR with fixed, enough (LD:ON +LD:OFF) time)

  (not con figurable with ONUs' capabilites, which is multi-instance-based and adds complexity)
  - **OLT capabilities (ATC, CDR time) report to ONUs in REGISTRATION message**
  - **OLT cap. Echo from ONUs in REGISTRATION_ACK message**
  - **ONU MAC signals PMD to turn on the LD at (prebias+ATC+ CDR time) ahead of Slot Start and to turn off the LD at (Slot Start +sum of Transmitted packet length)**

802.3z GbE timing-related spec.

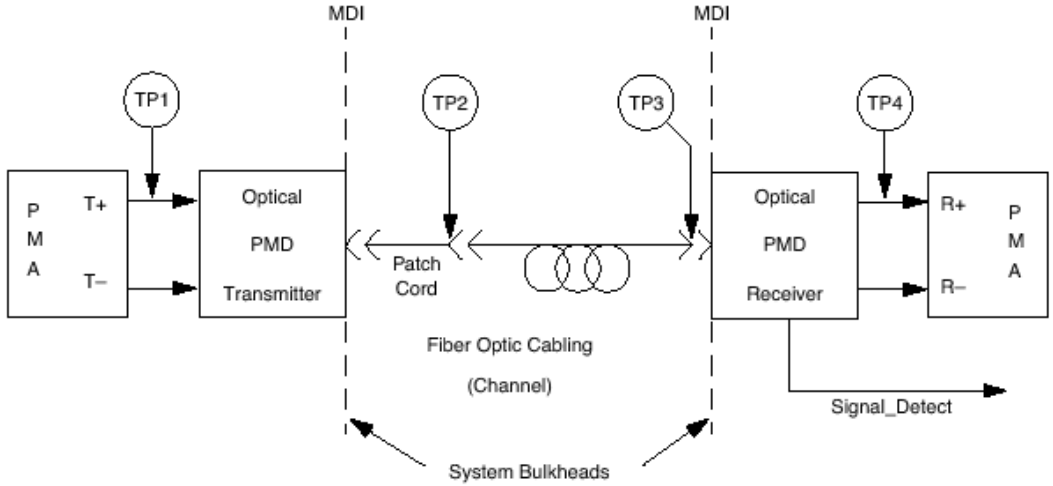


Figure 38–1—1000BASE-X block diagram

1000BASE-SX/LX jitter budget

Compliance point	Total jitter[1)]		Deterministic jitter	
	UI	ps	UI	ps
TP1	**0.240**	192	0.100	80
TP1 to TP2	0.284	227	0.100	80
TP2	**0.431**	345	0.200	160
TP2 to TP3	0.170	136	0.050	40
TP3	**0.510**	408	0.250	200
TP3 to TP4	0.332	266	0.212	170
TP4[2)]	**0.749**	599	0.462	370

Signaling speed : 1.25±100ppm(GBd)
Trise/fall (20-80%) : 0.26ns

1) Total jitter is composed of both deterministic and random components. The allowed random jitter equals the allowed total jitter minus the actual deterministic jitter at that point.
2) Measured with a conformance test signal at TP3 set to an average optical power 0.5dB greater than the stressed receive sensitivity from receive characteristics.

Clock drift and Jitter

- EPON has a global system clock
- Clock synchronization is instance-based, as local clock is set at the point of every GATE reception

  - robust to clock drift
- Tolerable clock drift is +- 100ppm when using GE Transc.

  for Rsv. Window size =2msec, Td = 400nsec

  when clock drift is +- 40pppm, Td = 160nsec (25 Octets)

  for 8000byte Grant_Length allocated to ONU,

  IFG=12 Octet, and GB=50 Octets

  BW Utilization = 0.709 (min. packet size) - 0.977 (max. packet size)

- Clock drift due to RTT change

  - with extended temperature optics -40 to 85^{o}C

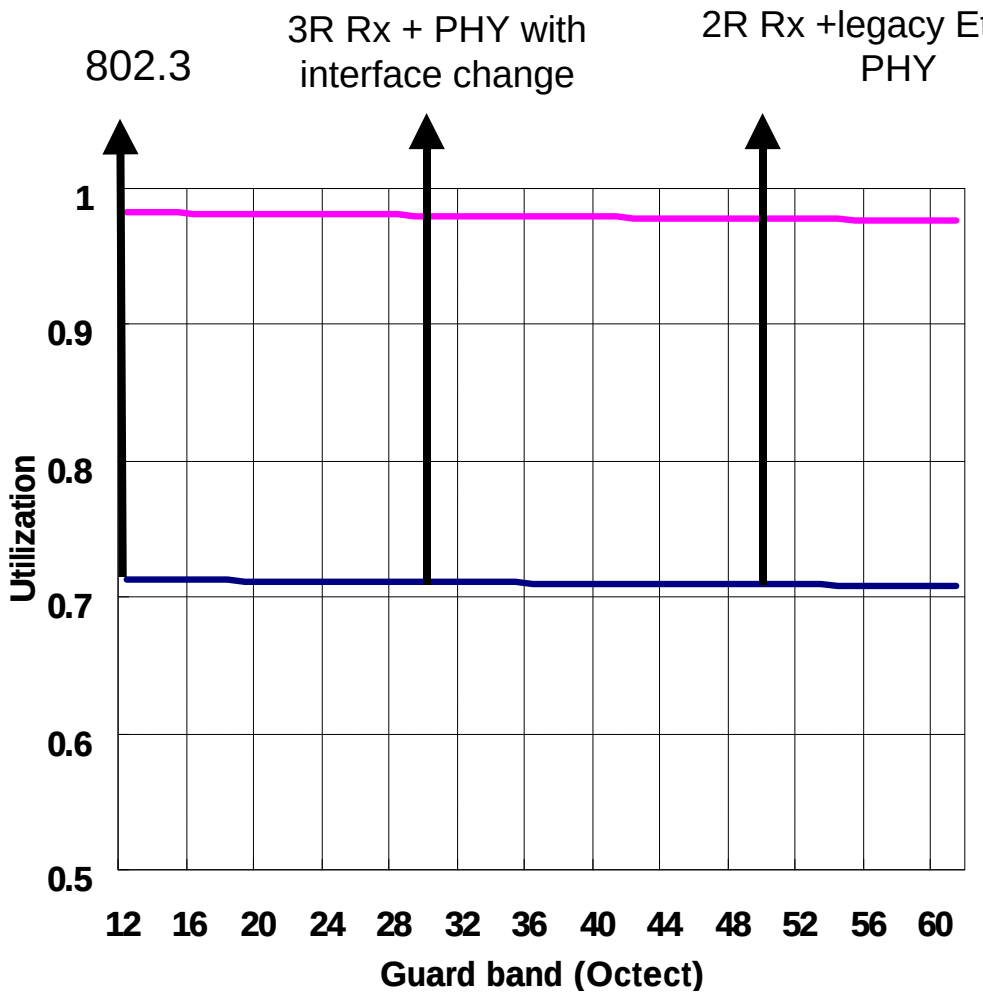
  RTT change coeff. is about 7ppm/ ^{o}C, which is forgiving within the Rsv. window

  If (OLT clock-ONU clock) > (threshold for clock mismatch) occurs over several consecutive windows , rerange the ONU for RTT calibration.

- guard band for 16bit clock resolution is 4 octets

- Jitter budget for EPON would be 0.749UI above 637kHz, and jitter tolerance, jitter transfer and generation are TBD according to device capability.

BW utility



IFG=12 Octets

8000byte BW Grant

Summary

- **Issues of embedded PHY parameters for MPCP**
- **Need to gather from vendors standard data for PMD timing parameters for modeling and performance evaluation**
- **Configurable with OLT's capability and universal spec for ONUs' capabilities for system scalability and centralized management**