

FEC in EPON Technical Proposal

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Scope

- ❑ **Sales pitch**
- ❑ **Frame format**
- ❑ **Frame synchronization algorithm and state machines**
- ❑ **Mean time to false packet acceptance**

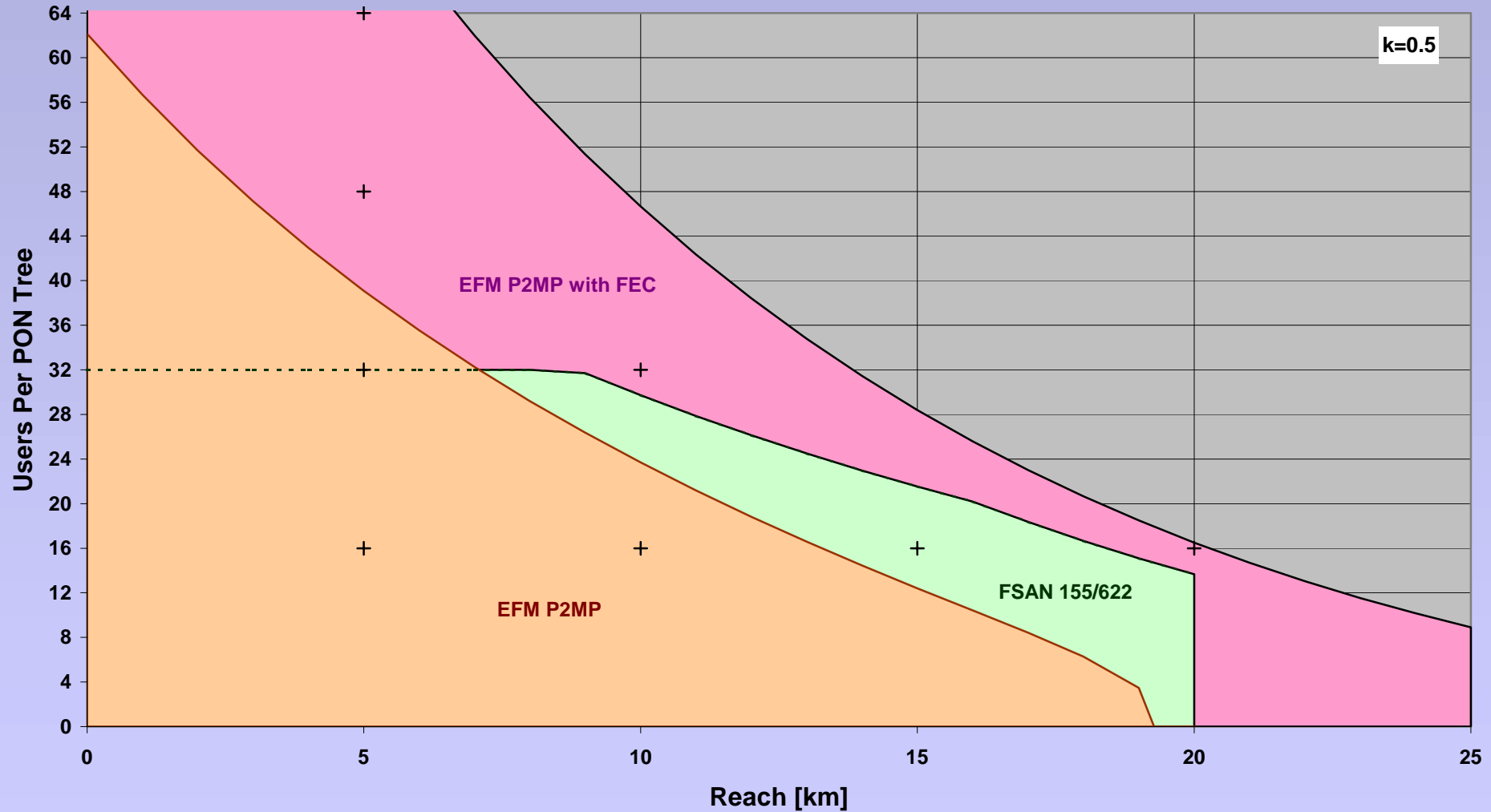
Motivation

- **Higher line rate in EFM PON causes split deficiency vs. APON**
 - Shuts out FTTH market

- **FEC is the cost effective method to meet reach/split targets maintaining low-cost optics**
 - Increase splits – when power limited
 - Increase distance – when MPN-limited

- **Improve Business Case**

Competitive With FSAN



k=0.5

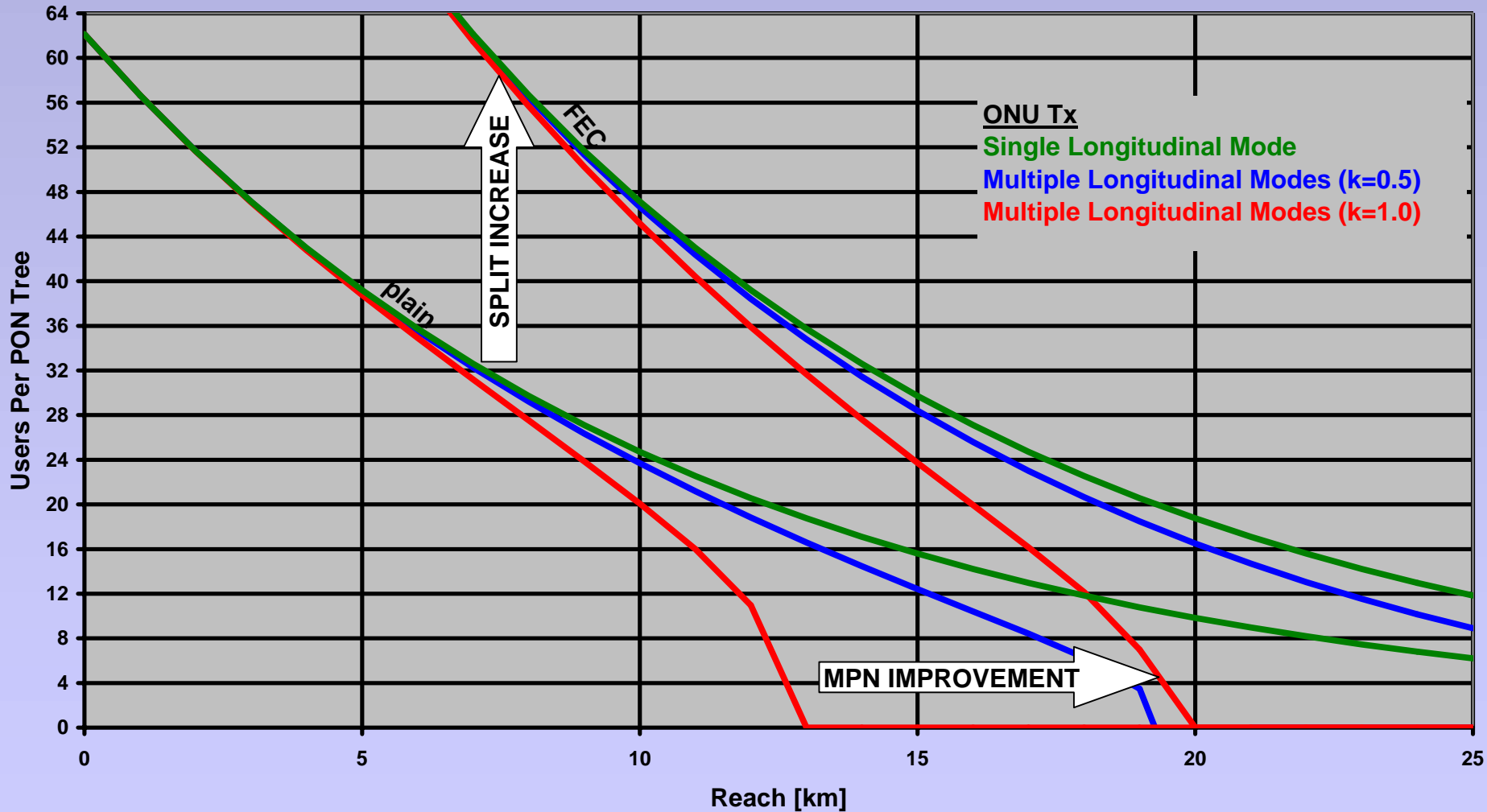
EFM P2MP with FEC

EFM P2MP

FSAN 155/622

What is the Gain?

P2MP PMD Proposal



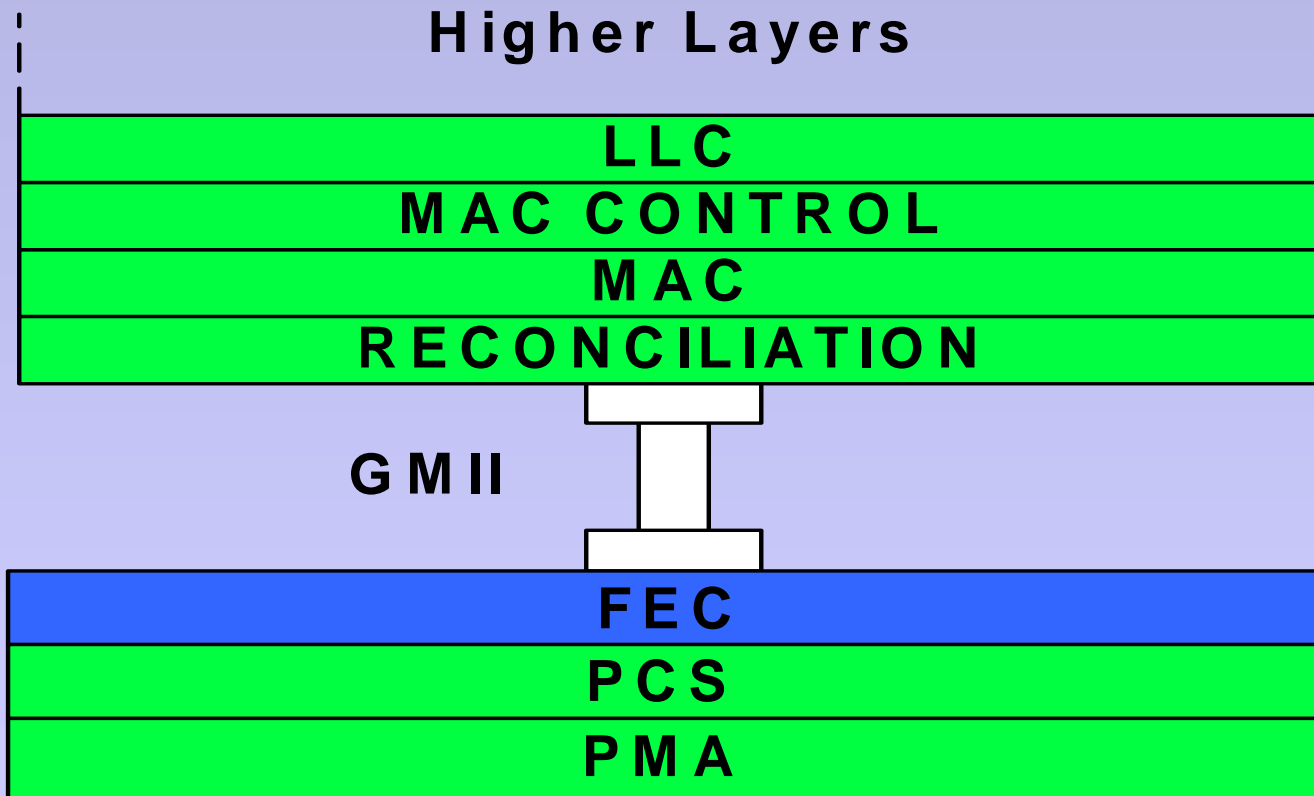
FEC Compatibility

- **Compatibility with legacy Ethernet format**
 - Network shared by FEC and non-FEC devices
 - FEC coding only for devices requiring it
 - Stream of an FEC coded data should be understood by current non FEC devices without undue errors
- **Ability to add FEC functionality externally**
 - ⇓
- **Optional and transparent use of FEC**

Basic Principles of Operation

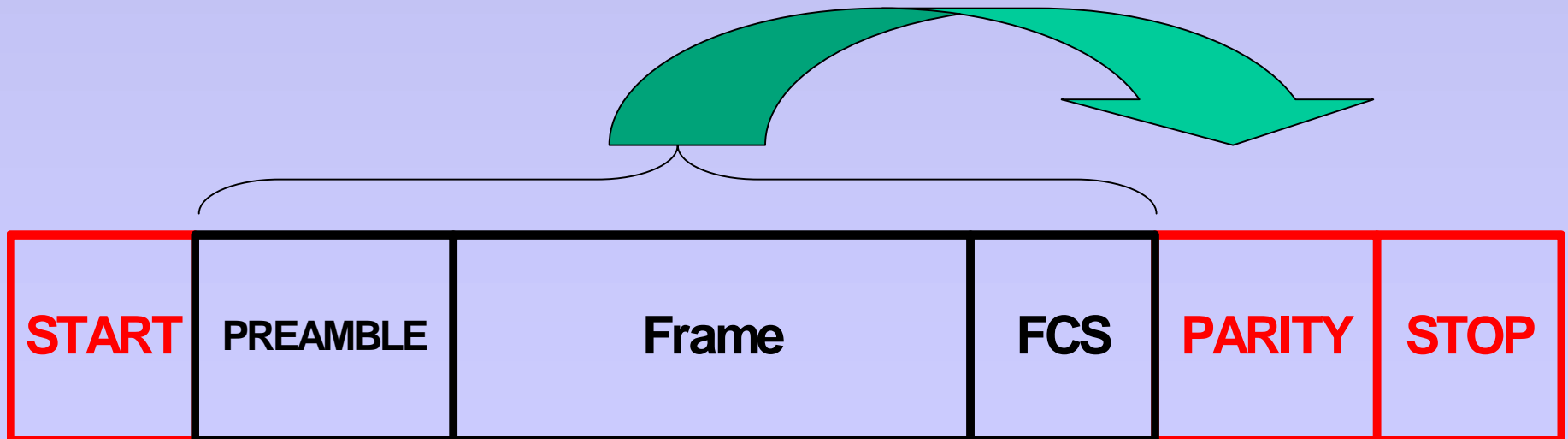
- **Maintaining the frame structure**
 - Parity check bytes added at the end of the frame
 - **FEC is coded before the 8B/10B code**
- ⇓
- **Legacy devices observe a normal Ethernet frame**
 - False_Carrier_detect mode of PCS Rx when parity bytes received (RX_ER is asserted)

FEC Layering in P2MP Ethernet



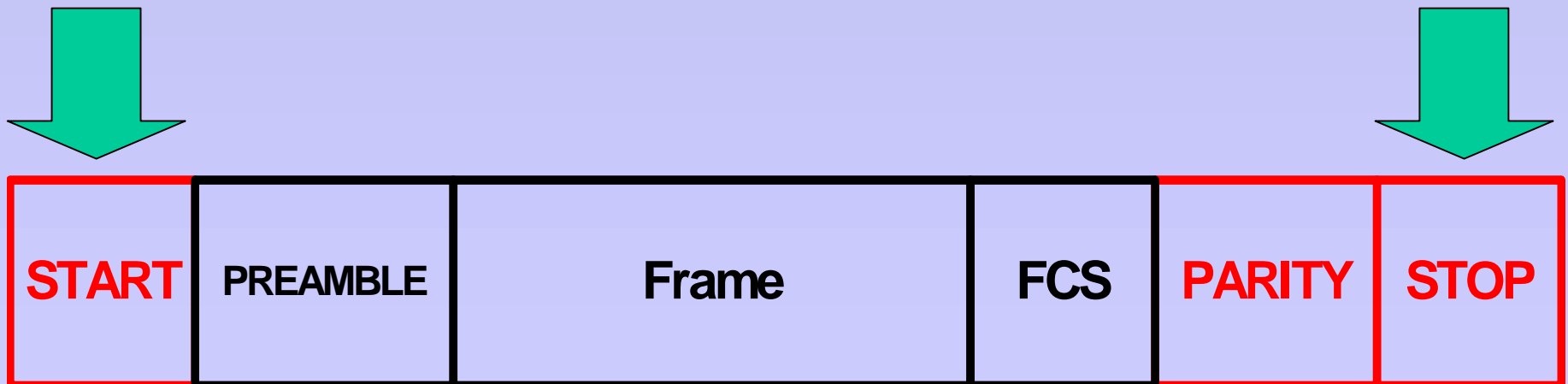
Encoding

- ❑ Parity check bytes added at the end of the packet
- ❑ All of the packet is encoded including preamble, address and FCS
- ❑ Shortened last frame – virtual zero padding
- ❑ Idles not protected



Frame Markers

- ❑ Special start and stop symbols added
- ❑ Symbols are immune to high noise
- ❑ Symbols are actually sequences detectable with a correlator
- ❑ 60 bit long for noise immunity



Protection Sequence Selection

- ❑ Sequence is long enough to be detected with very high probability
- ❑ Sequence can flow through non-FEC PCS transparently

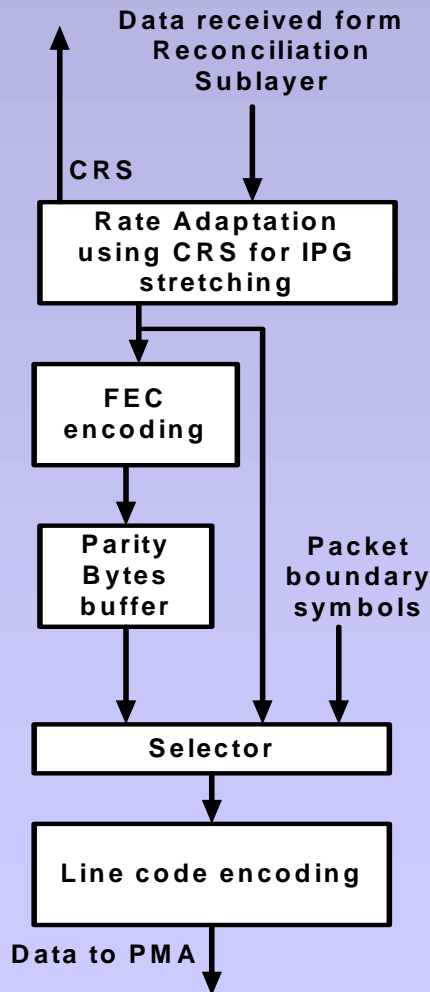
- ❑ **Examples**
 - /K28.5/ - comma is in the idle word and is duplicated many times – remains the same
 - /S_fec/ - Start_of_Packet - ex: /R/R/K28.5/D5.6/S/
 - /T_fec/ - End_of_Packet - ex:
/T/R/K28.5/D21.2/T/R/

FEC Rate Adaptation

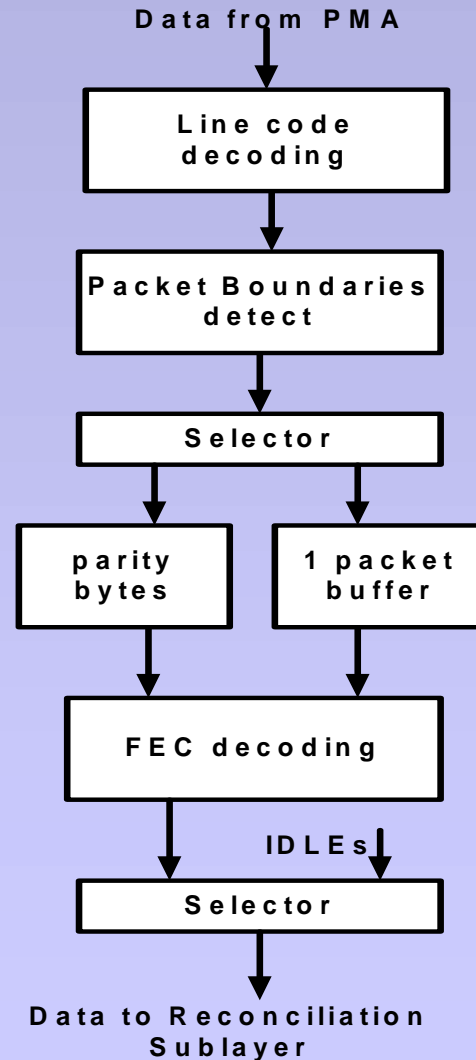
- **Additional idles inserted in FEC packet reception instead of additional data**
- **In transmission rate adaptation can be achieved in 2 ways**
 - Open loop - IPG stretching adapting MAC rate
 - Close loop – exporting a signal from PHY to the reconciliation layer
 - CRS or COL lines existing in half duplex mode

Data Flow for FEC Sublayer

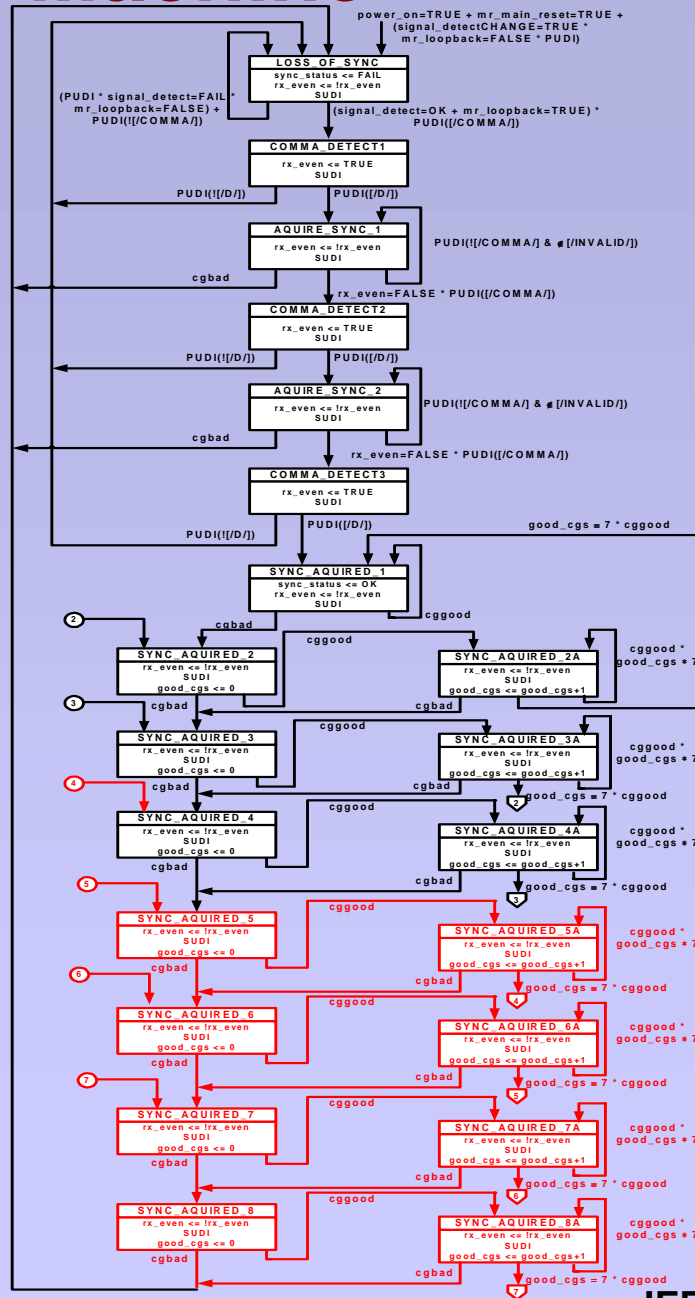
Packet Tx FEC Encoding



Packet Rx FEC Decoding



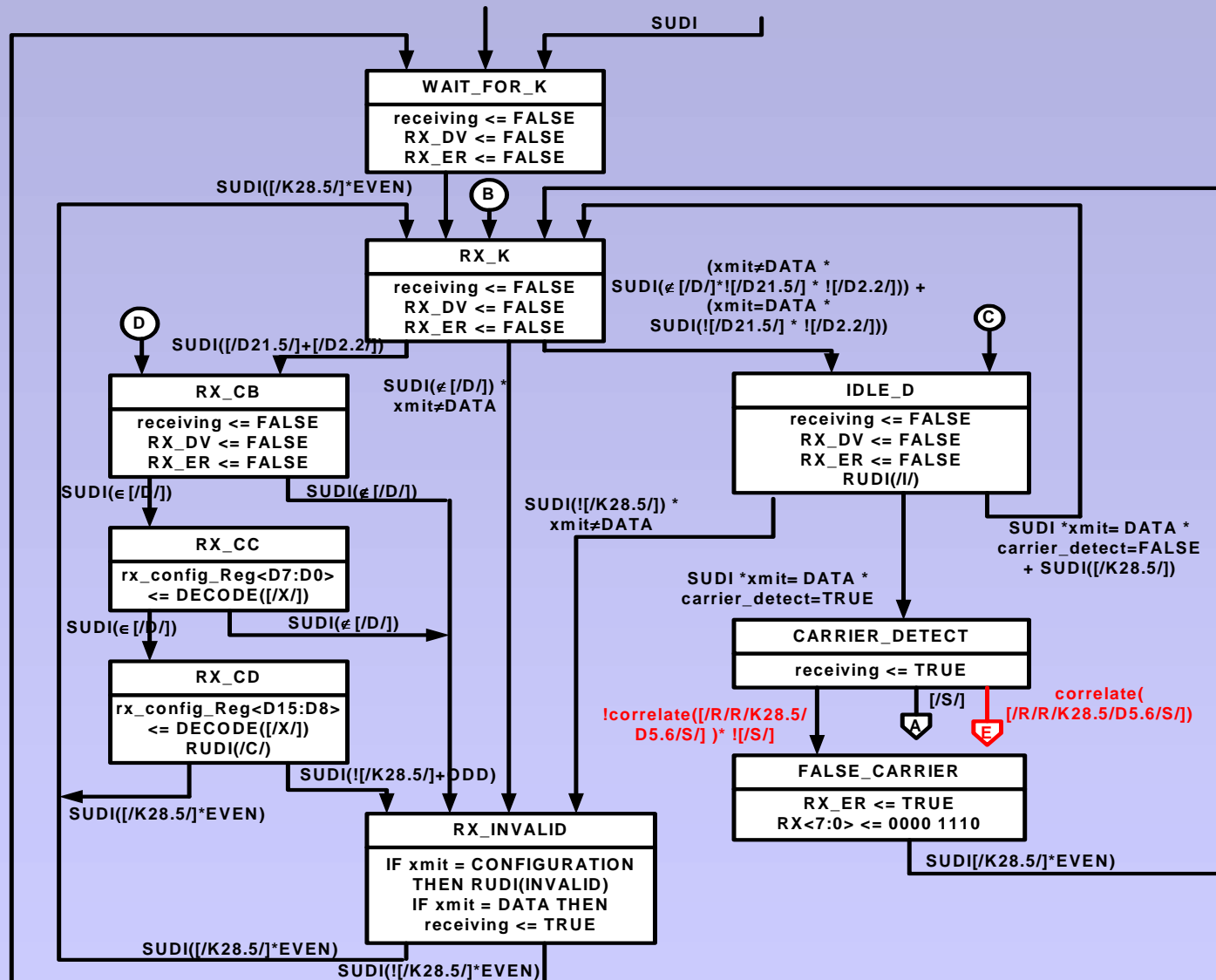
Rx Sync State Machine



Probability for Lock Errors

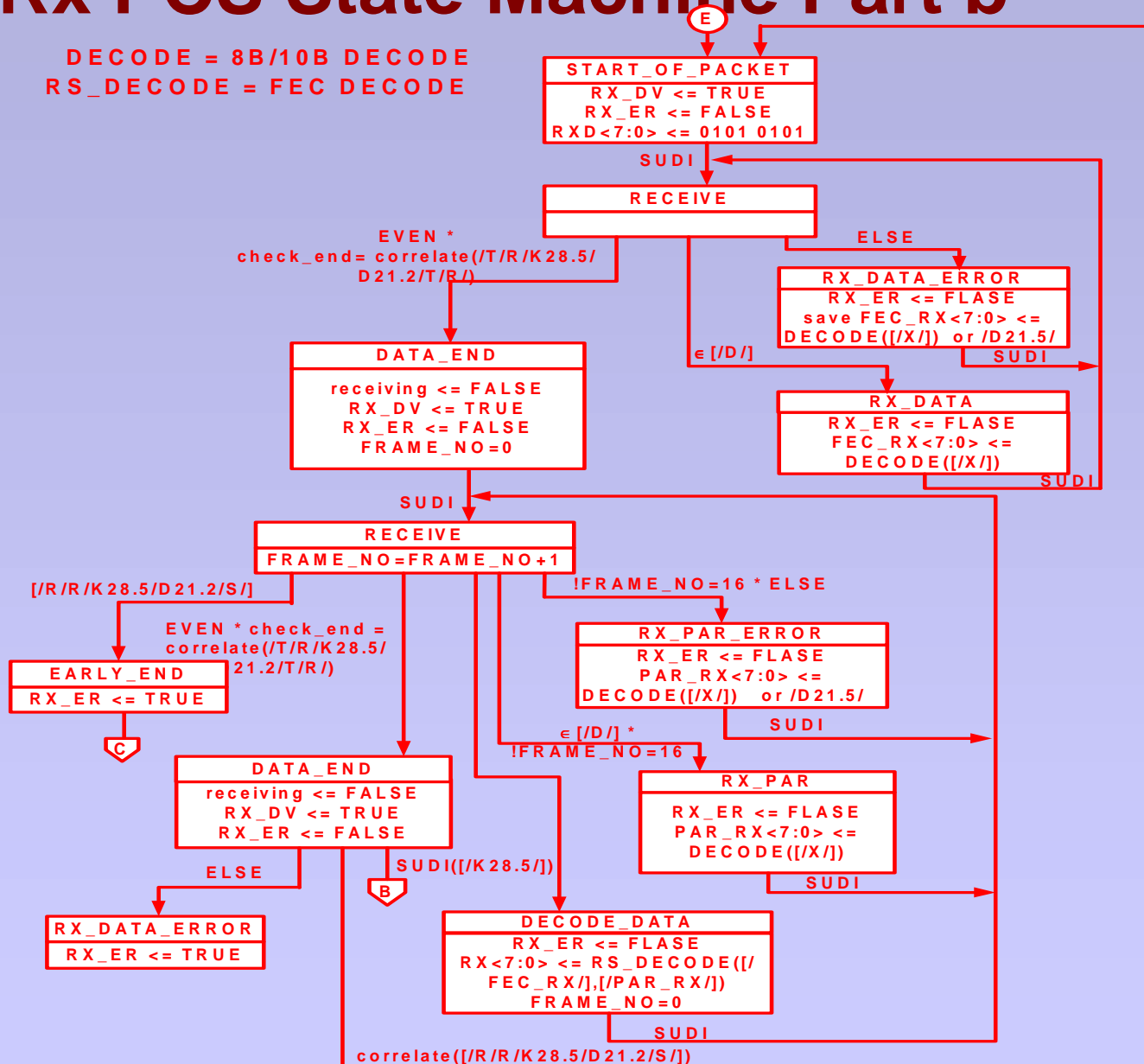
- ❑ Acquisition is performed following 3 commas detection. Acquisition error probability is reduced from $3e-11$ to $3e-3$
- ❑ De-acquisition – following 3 sequential bad words – reduced from $(1e-11)^3$ to $(1e-3)^3$ – once every 1sec
- ❑ 7 step state machines reduce the probability to $(1e-3)^7$ – one in every 31,700 years

FEC Rx PCS State Machine Part a



FEC Rx PCS State Machine Part b

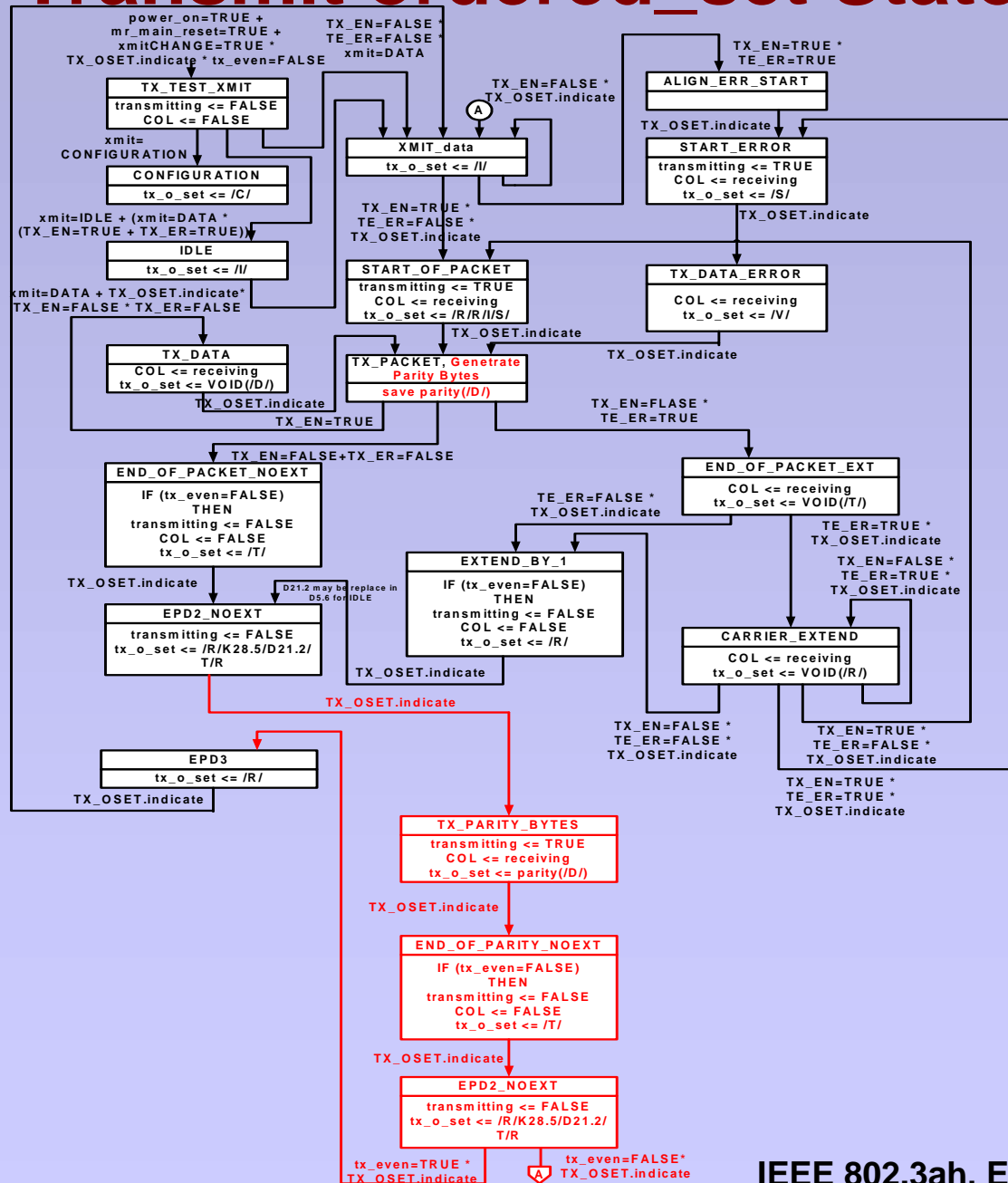
DECODE = 8B/10B DECODE
 RS_DECODE = FEC DECODE



PCS RX State Machine

- ❑ Only Frame boundary detection is added to current PCS Rx State Machine
- ❑ FEC detection is independent and performed above the current PCS Rx State Machine

FEC PCS Transmit ordered_set State Machine



Mean Time to False Packet Acceptance

- Bit error probability before FEC is $P_e=1e-4$
- Bit error probability After FEC is $P_{cu}=1e-12$
- The probability for an FCS error in Ethernet:

$$P_{UD} = \frac{1500}{255} \cdot \frac{P_{CU}}{10} \cdot \left(\frac{1}{2}\right)^{32} = 1.4e - 22$$

- Most code-words are not 17 bytes distant The number of 17 bytes neighbors:

$$R_{17} = \frac{\binom{17}{9} \cdot A_{17}}{\binom{255}{9} \cdot (256)^9} = \frac{\binom{17}{9} \cdot \left[\binom{255}{17} \cdot 255 \right]}{\binom{255}{9} \cdot (256)^9} \approx 6 \cdot 1e - 8$$

Mean Time to False Packet Acceptance

– Cont'

- Total probability of undetected errors for Ethernet with FEC – $1e-29$
- For 1GE this means an error in $4e16$ years

Miss detect in Start & Stop Markers

- Length of correlation sequence – 6 bytes that are 60 bits – detected with bit correlators
- Probability of miss-detect from IDLE pattern

– The minimal distance of a sequence from an IDLE pattern is 15 bits –

$$P_{ce} < \binom{15}{7} P_b^7 \approx 1e - 24$$

- Probability of miss-detect from IDLE pattern

– The nearest data sequence is 6 bits distant -

$$P_{ce} < \frac{320}{(2^8)^6} \cdot \binom{6}{3} P_b^3 \approx 2e - 23$$

Conclusion

- ❑ **FEC framing compatible with legacy Ethernet introduced**
- ❑ **Layering proposed above PCS with PCS extensions**
- ❑ **Frame format uses IPG for code words**
- ❑ **Low probability of error propagation shown**
- ❑ **60 bit patterns used as markers**
- ❑ **Two minimally intrusive schemes for MAC integration shown**