Burst Mode Technology

A Tutorial

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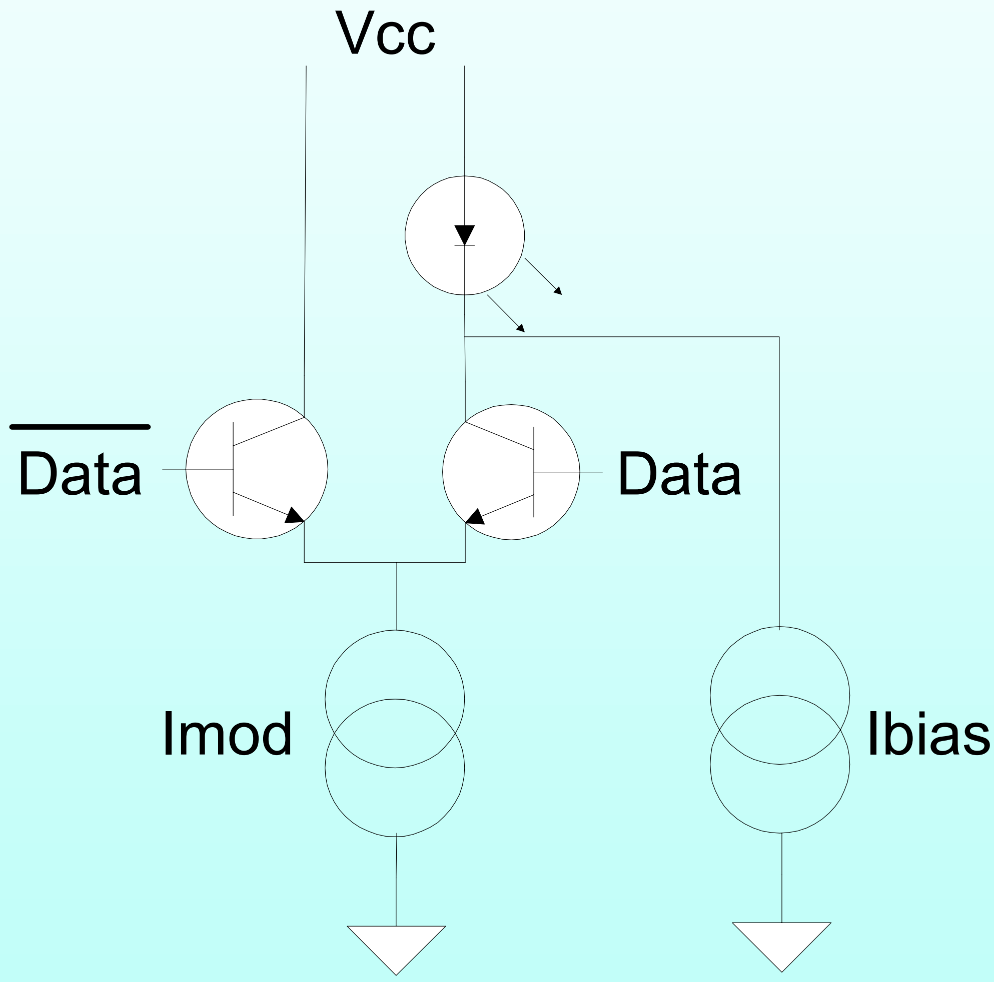
Overview

- *Burst Mode Transmitters*
  - *Rise and fall times*
  - *Automatic power control*
- *Burst Mode Receivers*
  - *Several approaches to level recovery*
  - *Fast clock recovery*
  - *Delimiters and error tolerance*

Rise and Fall times

- *Conventional circuits are designed to maintain a constant bias current*
- *No attention was paid to being able to change the bias current quickly*
- *It is no surprise that some conventional circuits have very poor performance*
- *However, some conventional circuits have pretty good performance*

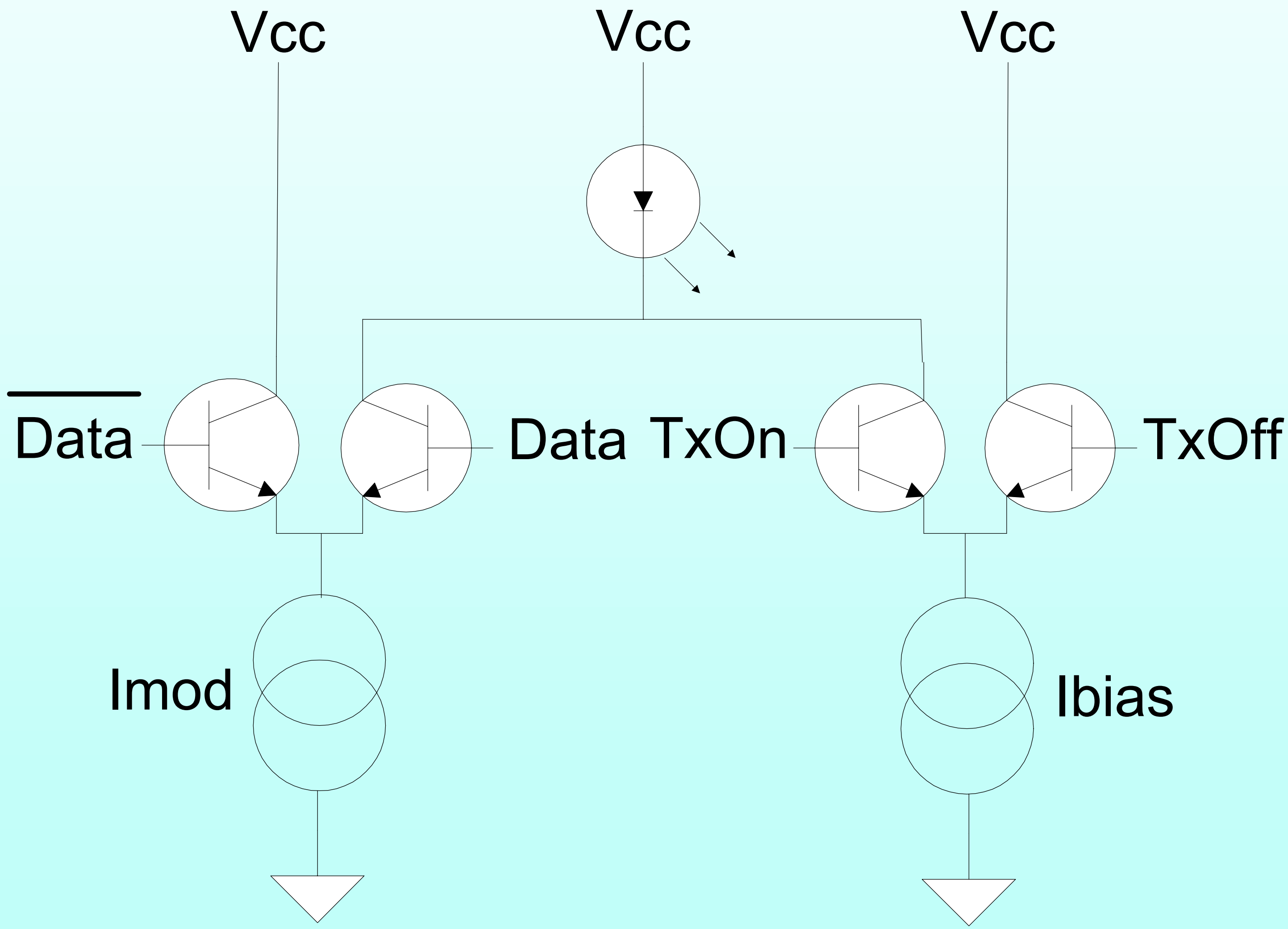
Conventional laser driver



Positive solution to problem

- *Simple argument: if you can build a circuit that can modulate the diode at the bit rate, then you must also be able to modulate the bias current at the same speed*
- *Existence proof is following circuit*

Burst mode laser driver



Basic Take-away Message

- *Laser driver circuits can be designed that have short Ton and Toff performance*
  - *155 Mb/s systems have Ton=Toff=6.4ns*
- *Such devices carry little to no complexity premium over 'standard' drivers*

Automatic power control

- *Conventional circuits often use*
  - *Slow monitor photodiode*
  - *Analog filters to average signal*
  - *Analog control loop to maintain desired operating point.*
- *Burst mode prevents the use of simple analog control loops*

Digital Burst APC

- *Monitor diode output is sampled at appropriate points in burst waveform*
- *Samples drive digital control loop*
- *Drive outputs are stored in memory for 'instant on' capability*
- *Such a scheme can be built using a cheap micro-controller device*

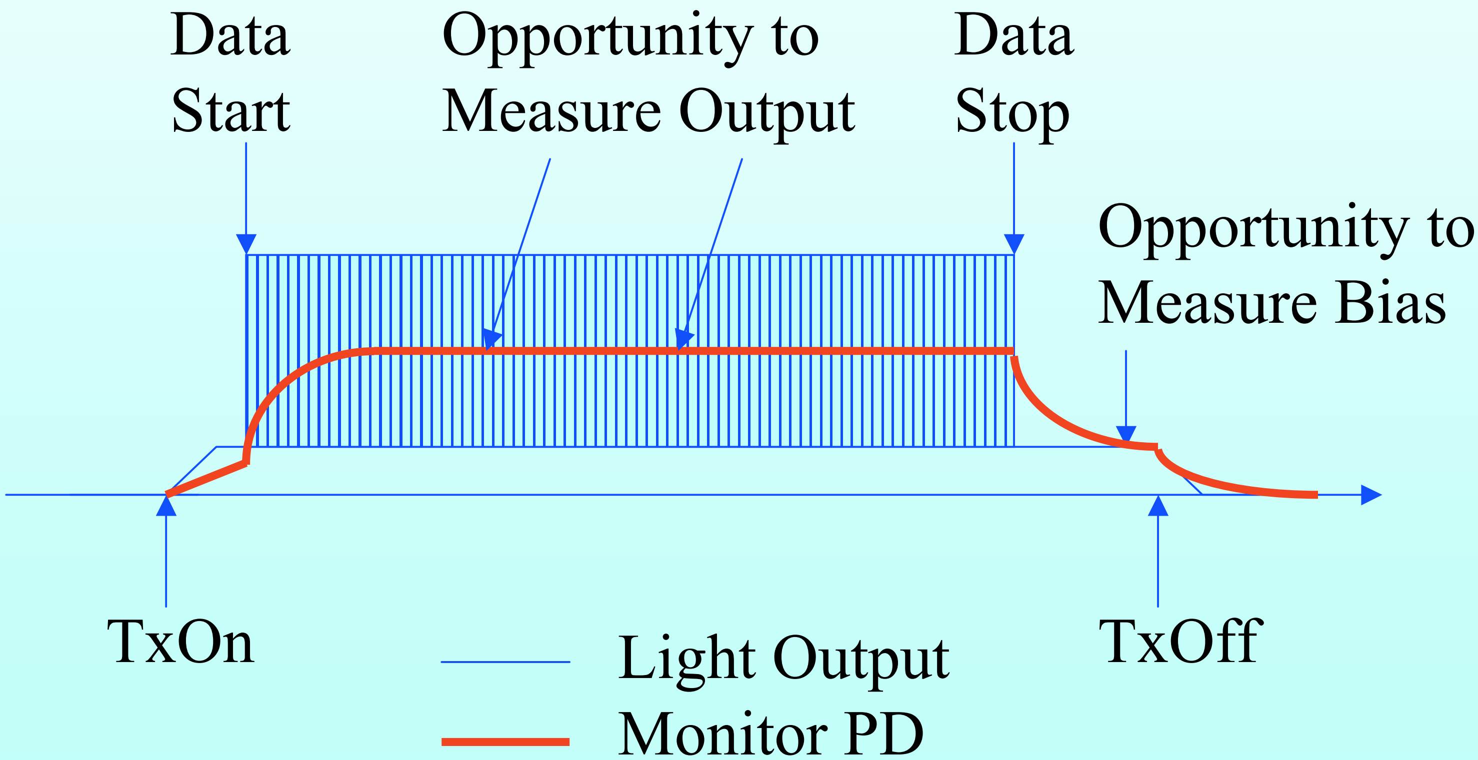
Extinction Ratio Control

- *Ideally, APC should maintain ER as well as average power*
- *Given enough 'structure' in the physical layer overhead, this can be done*
- *Power control fields that are all zeros or all ones allow the slow monitor to accurately measure these levels*
- *Digital control takes care of the rest*

Example of Tx control

- *At end of burst, when no more data is to be sent, a Tx control sequence can be sent*
- *Tx control is a block of all-zeroes*
- *The length of the block determines the required speed of the monitor diode*
- *The OLT doesn't see this signal*
- *Would require an extra 'signal' from the MAC to the PMD to start Tx control*

Example of Burst with Transmitter Control Appendix



Overview

- *Burst Mode Transmitters*
  - *Rise and fall times*
  - *Automatic power control*
- *Burst Mode Receivers*
  - *Dynamic Sensitivity Recovery*
  - *Level Recovery*
  - *Fast Clock Recovery*
  - *Delimiters and error tolerance*

Dynamic Sensitivity Recovery

- *A weak burst following a strong burst is hard to see*
- *The recovery process is limited by:*
  - *Photodiode carrier transport effects*
  - *Amplifier slew and charging rates*
  - *Unintentional "AGC" effects*

Photodiode Effects

- *A good PIN is actually quite linear*
- *Some PIN diodes are made so that light can stray into low field regions of the junction*
- *Carriers generated there are slow, and lead to a long tail in time response*
- *The solutions include*
  - *Only use diodes that don't have the 'tail'*
  - *Use an AC-coupled level recovery scheme*

Amplifier Slew Rate

- *The analog chain must settle quickly*
- *Limitations are mainly RC time constants*
- *Solutions are: decrease R and C*
- *Integration helps to reduce C*
- *An analog 'reset' can momentarily reduce R, substantially accelerating recovery*

Unintentional AGC

- *In general, a good burst mode pre-amplifier should have a simple transfer function, and no 'memory'*
- *Many pre-amps exhibit slow gain compression characteristics*
  - *This is great for continuous mode*
  - *This is the kiss-of-death for burst mode*
- *Solution: choose your amp wisely*

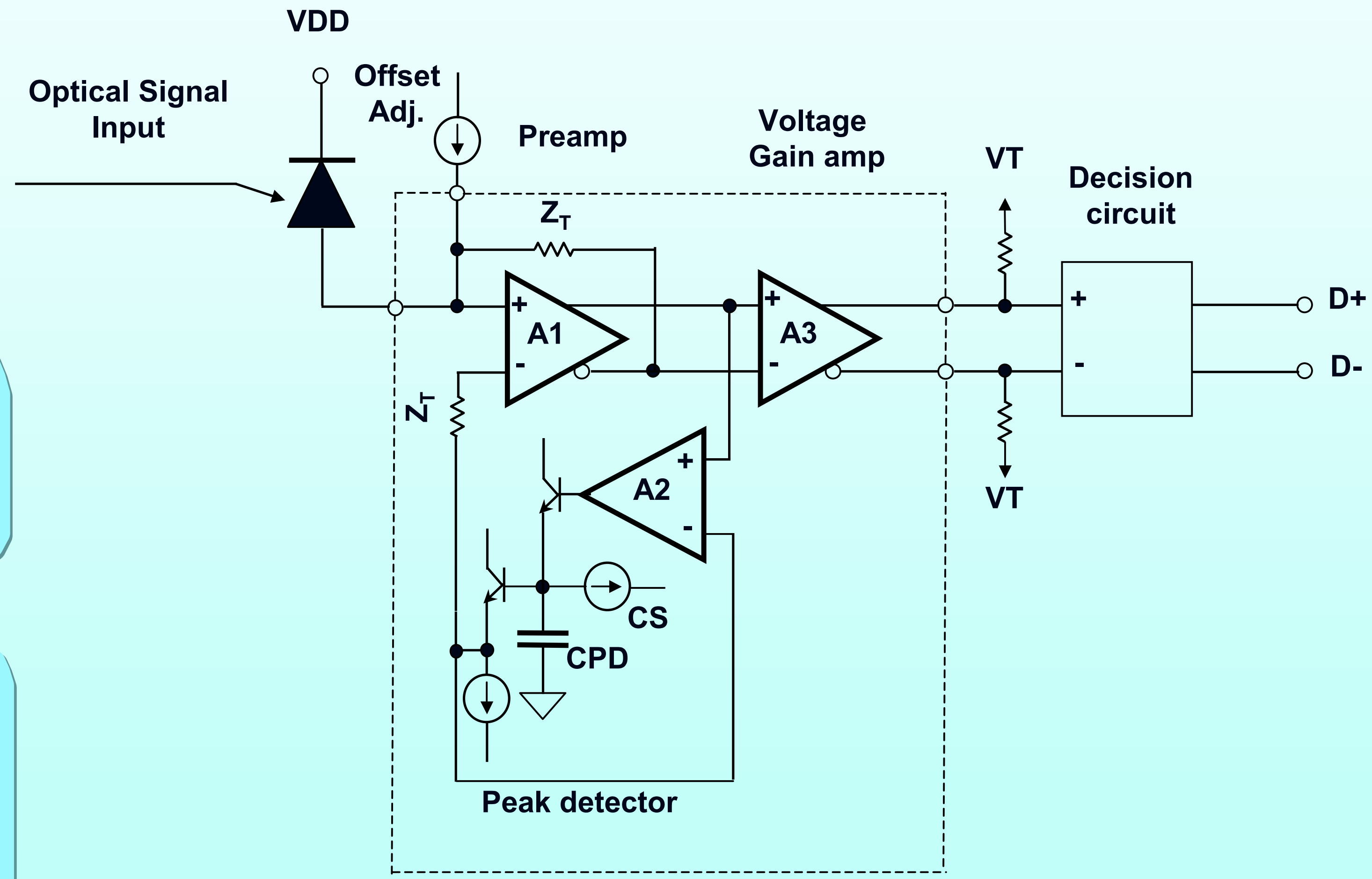
Receiver Level Recovery

- *The first challenge is to restore the logic levels to the burst mode signal*
- *DC coupled methods*
  - *Feedback (automatic gain control)*
  - *Feedforward (automatic threshold control)*
- *AC coupled methods*
  - *Frequency domain (analog filters)*
  - *Time domain (differential delay receiver)*

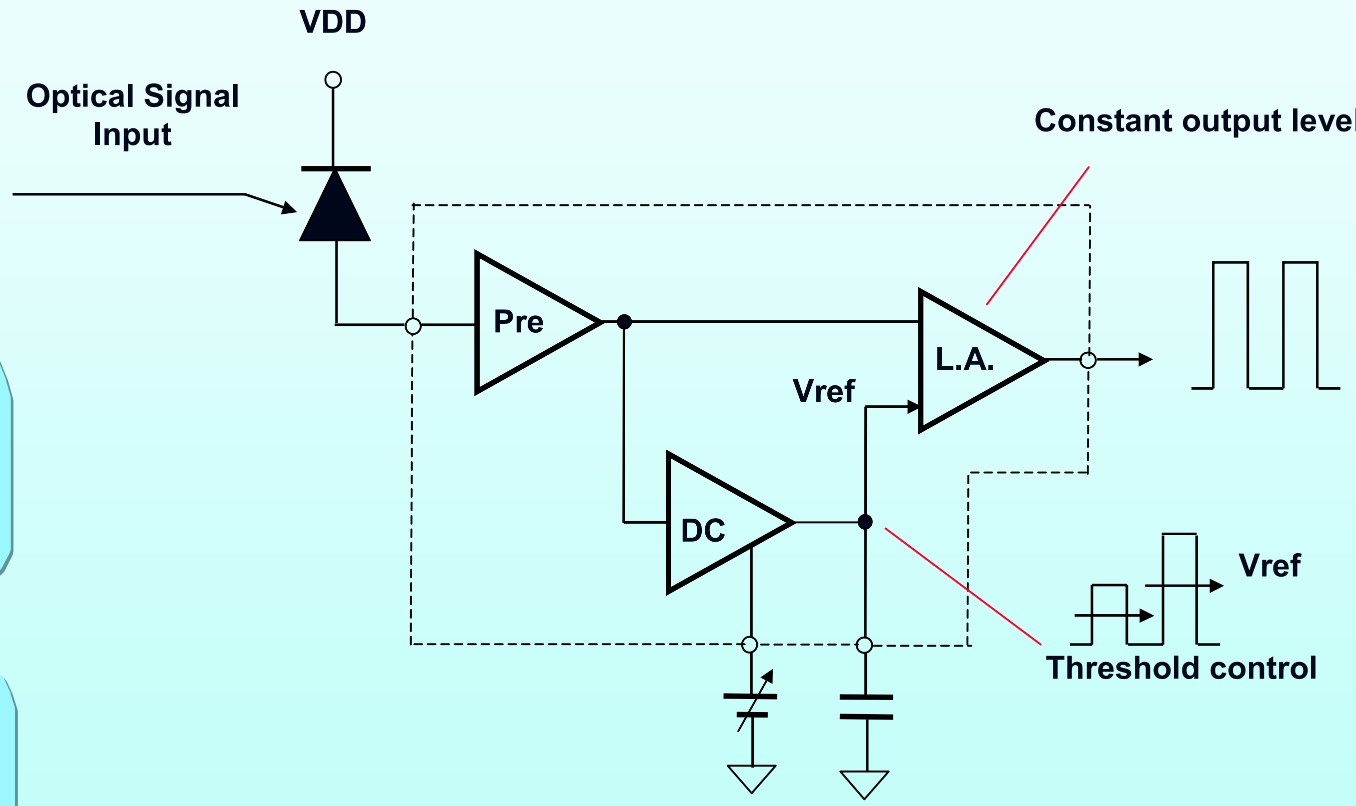
DC methods

- *Concept is simple: when each burst comes in, measure its power levels, and adjust accordingly*
- *Implementation requirement: signal path must be linear and DC coupled up to decision circuit*
- *Theoretically, this approach has low burst mode penalty*
- *Can be limited by nonlinear decay elements (like poor amplifiers or slow photodiodes)*

Feedback Topology



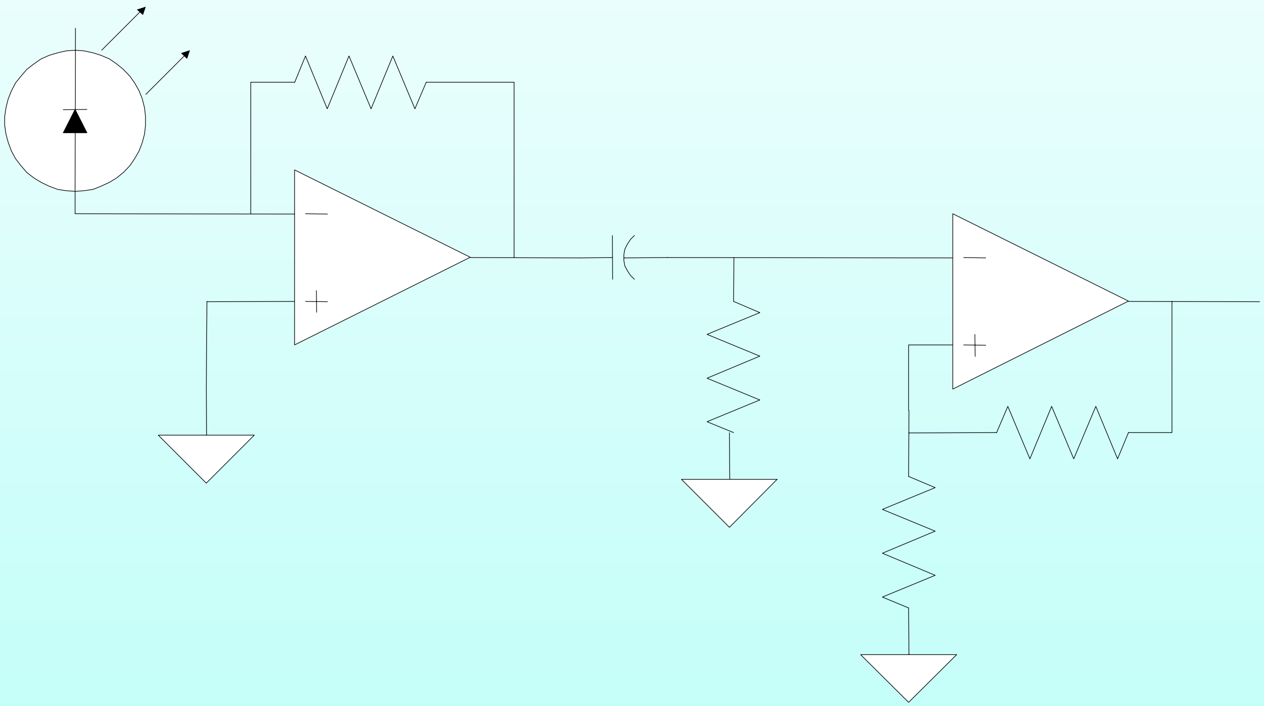
Feed-forward Topology



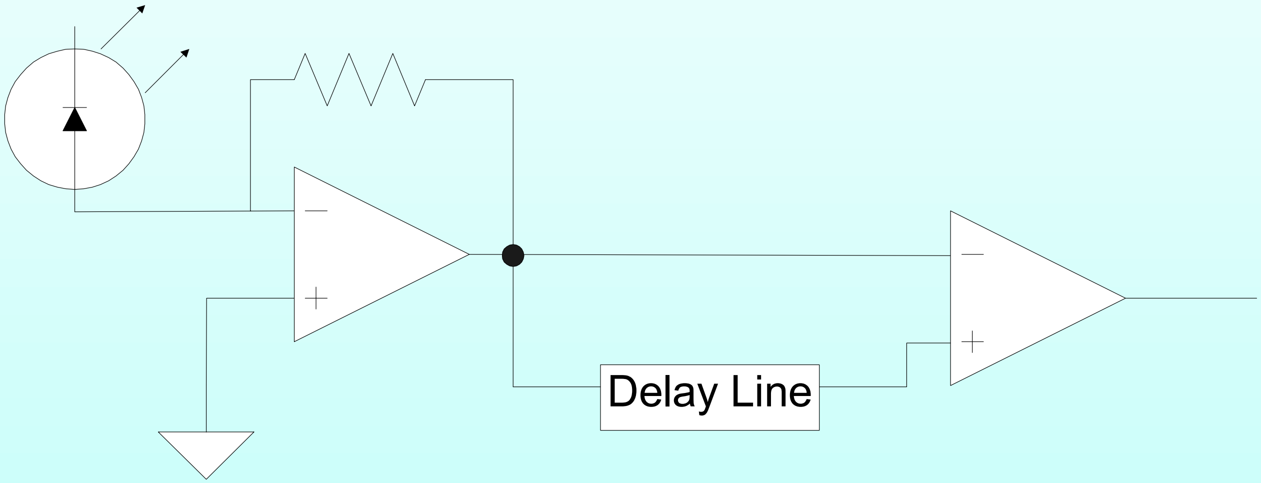
AC methods

- *Basic concept: Make the Rx channel so that it rejects the burst-to-burst level shifts while maintaining signal integrity*
- *A high-pass filter does the job*
  - *Level shifts are relatively slow signals*
  - *Data bits are relatively fast signals*
- *Theoretically, this approach carries a small sensitivity penalty (~1.5dB)*
- *Good rejection of all slow decaying signals*

Frequency domain filter

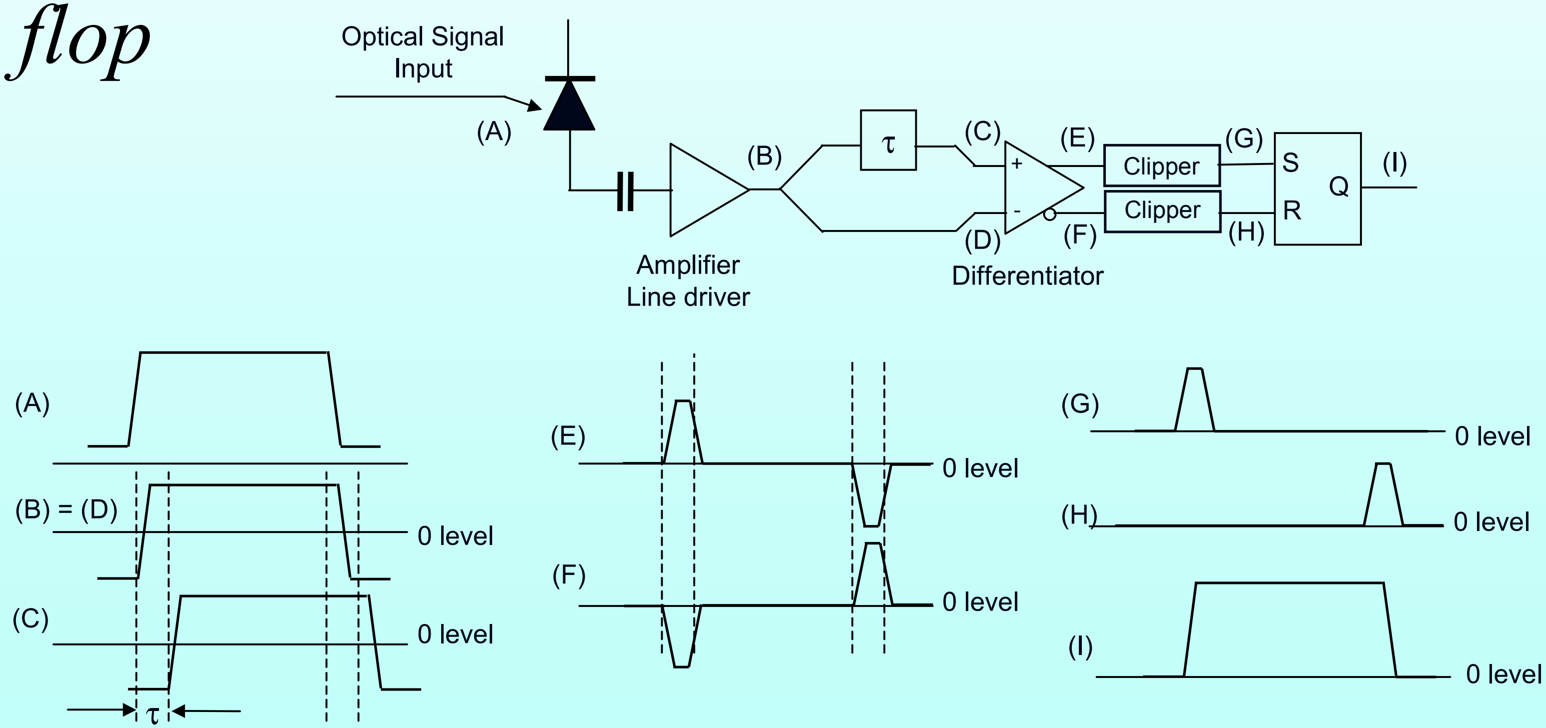


Time domain filter



Restoration of data

- *In the case of short time constants, the AC coupled output is a tri-state signal*
- *Data can be regenerated by use of a flip flop*



Measured performance

- *DC based schemes at gigabit rates have been reported as 8~40 ns for total Tlr + Tdsr*
- *Frequency domain AC schemes at 622 rates have been measured at 8 ns for total Tlr + Tdsr*
- *Time domain AC schemes can approach single bit duration recovery times*

Fast Clock Recovery

- *Classical clock recovery (PLL) does not work well*
- *Clock recovery falls into general classes*
  - *Oversampling in time*
  - *Oversampling in space*
  - *Instant locking*

Oversampling in time

- *Works by sampling the signal at several times the bit rate*
- *Best sample is selected by comparing to known good pattern (preamble)*
- *Becomes impractical at high rates*
  - *Gb/s bit rate would require ~5 Gsamp/s*

Oversampling in space

- *Works by generating several copies of the clock, each delayed by a different phase*
- *Best re-timing phase is determined by comparing outputs to known good pattern*
- *Approach is scalable*
- *Requires low-clock skew circuits*

Instant locking

- *Works by triggering the local clock on each incoming data transition*
- *Local clock carries system through periods of no transitions*
- *Approach is scalable*
- *Has a susceptibility to transient pulse distortions*

Burst Delimiter

- *Signal is used to find the logical start of burst*
- *Provides fast protocol synchronization*
  - *Standard synch methods don't work*

Analysis method

- *The delimiter problem is equivalent to finding the true delimiter symbol from the set of symbols arising from time shifted segments of the preamble-delimiter sequence*
- *The discrimination of code symbols in the presence of errors can be described by the Hamming distance*
- *The error resistance of a delimiter symbol is equal to N errors if its minimum Hamming distance is 2N+1 from all other symbols*

Robustness needs and limits

- *How robust must a delimiter be?*
  - *Assume the raw BER is 1e-4*
  - *Assume delimiter lengths of 8 to 20 bits*
- *At least 3 bit errors must be tolerated so that burst error rate is <1E-12*
- *Delimiter should have Hamming distance of 7*
- *How robust could a delimiter be?*
  - *Assuming a preamble that is 1010 repeating pattern*
- *A delimiter of 2N bits can have a minimum Hamming distance no greater than N from the preamble*

Results 1

- *Maximal Minimum Hamming distances computed for a selection of delimiter sizes via exhaustive search of all Delimiters*
- *Number of "Good delimiters" was found*
  - *Good Delimiter has maximal minimum distance*
  - *Good Delimiter has equal number of 1's and 0's*

Delimiter Length (bits)	*Maximal Minimum Distance*	*Number of Good Delimiters*
8	*3*	*17*
12	*5*	*78*
16	*7*	*311*
20	*9*	*713*

Results 2

- *The set of "Good delimiters" can be further reduced by finding those with a minimum number of low weight distances from other symbols*
- *These could be described as the "Best delimiters"*
- *For 8 bit delimiters, there are 7 such codes:*
  - *1B, 27, 2D, 8D, 93, D8, E4*
- *For 16 bit delimiters, there are 5 such codes:*
  - *85B3, 8C5B, B433, B670, E6D0*
- *For 20 bit delimiters, there is 1 such code:*
  - *B5983*

Summary

- *Burst mode technology is not new*
  - *Large volume of scientific literature*
  - *Many systems have reduced it to practice*
- *Using these design principles, one can achieve good performance for no extra cost*
- *Interested parties should work together on finding consensus values*