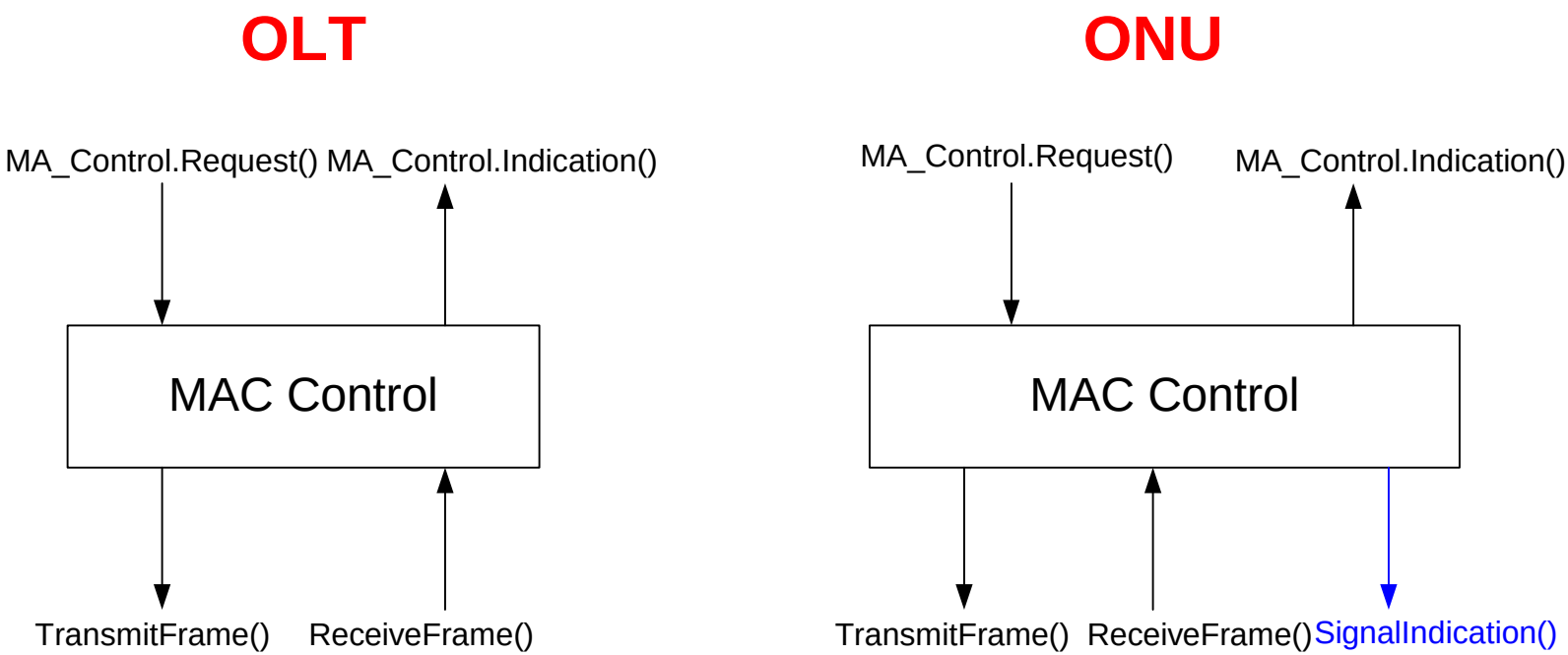
MPCP
A Timing Approach

Ajay Gummalla, Dolors Sala, John Limb – Broadcom

MPCP Framework



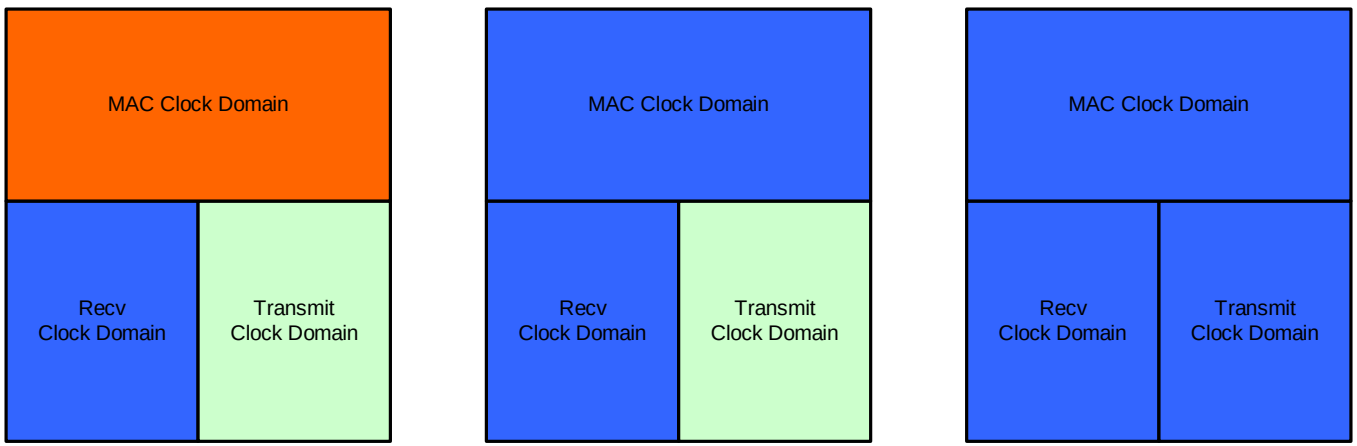
- **Multipoint extension based on MAC-control service interface and an additional SignalIndication to control burst mode**

Timing Function

- **MPCP is based on a Gate/Response mechanism**
- **Establishes a common time reference between OLT and ONUs**
  - Reference is necessary to determine when the ONUs may transmit without overlap

Clock Domains

- **All elements within a clock domain are based on a single clock and are frequency/phase locked.**
  - Counters are incremented/decremented using this clock



Asynchronous Clock Domain

Downstream Clock Domain

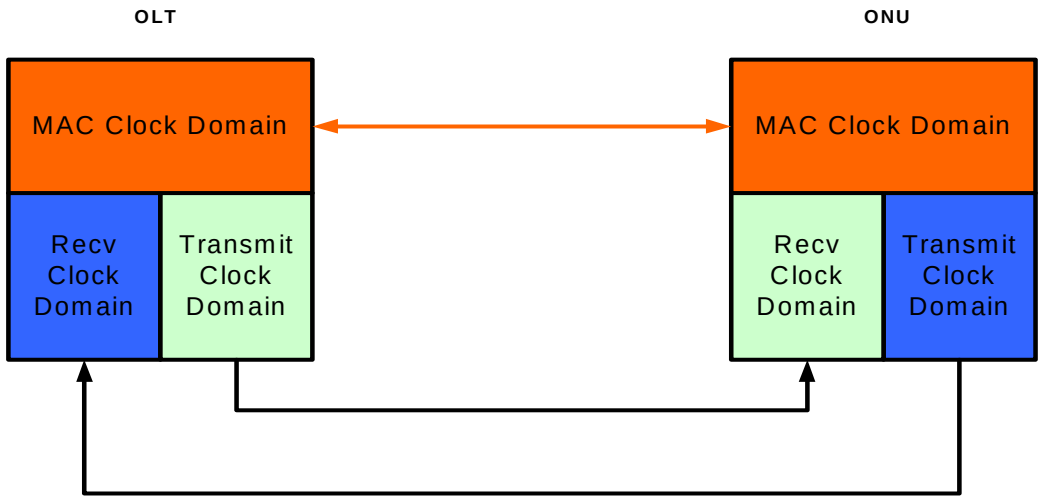
Synchronous Clock Domain

Timing Inaccuracies

- **Uncertainty in timing needs to be accounted for in the guard band**
  - a) Jitter from clock domain shifts
    - Uncertainty in phase of two clocks running asynchronously
  - b) Jitter from worst case clock drift
    - Worst case clock offset: 200 ppm (200 KHz)
    - Ex: counter that needs to count 1ms can be off by 200 bits
  - c) Jitter (not delay) from the time message is transmitted to when it is received
    - When messages contain time values, the variability in delay that should be accounted for in guard time
  - d) Jitter in message processing time
    - Jitter of software implementations can be in 100's of microsecs to millisecond
    - Jitter of hardware implementation can be negligible

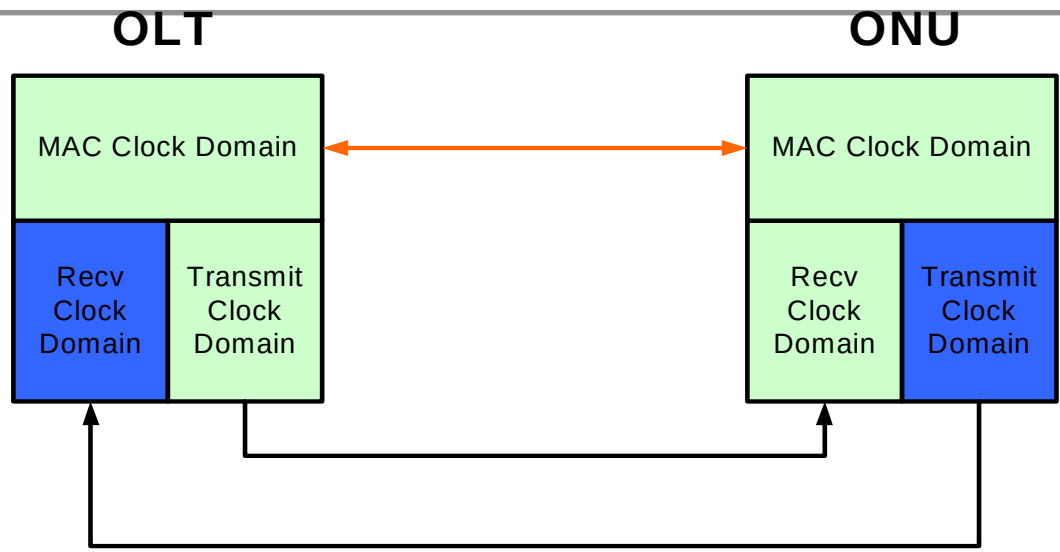
Only protocol component of the guard time described here

Asynchronous Clock Domain



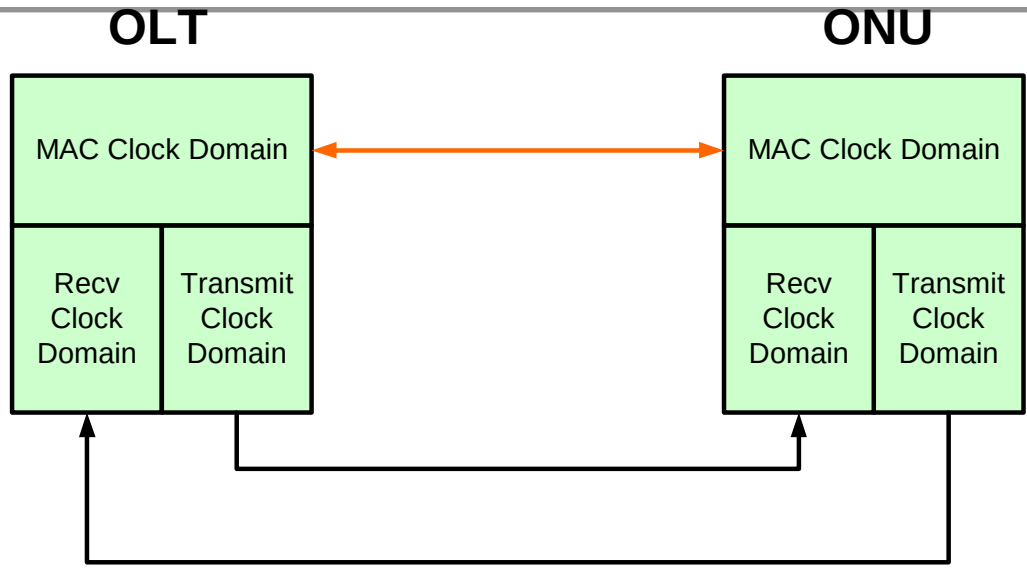
- MAC, transmit and receive clocks are independent
  - All timing uncertainties should be accounted for in guard band (a,b,c,d)
  - OLT and ONU MAC clocks can be synchronized accurately using frames
    - Eliminates jitter from worst case clock offset
    - Allowable guard band determines frame frequency

Downstream Clock Domain



- MAC Control operation in OLT is locked to its transmit phy clock
- MAC Control operation in ONU is locked to its receive phy clock
- OLT and ONU are synchronized through the receive bit/byte clock
- Only have to account for
  - **clock domain shift on transmit**
  - **clock drift for the transmit duration**

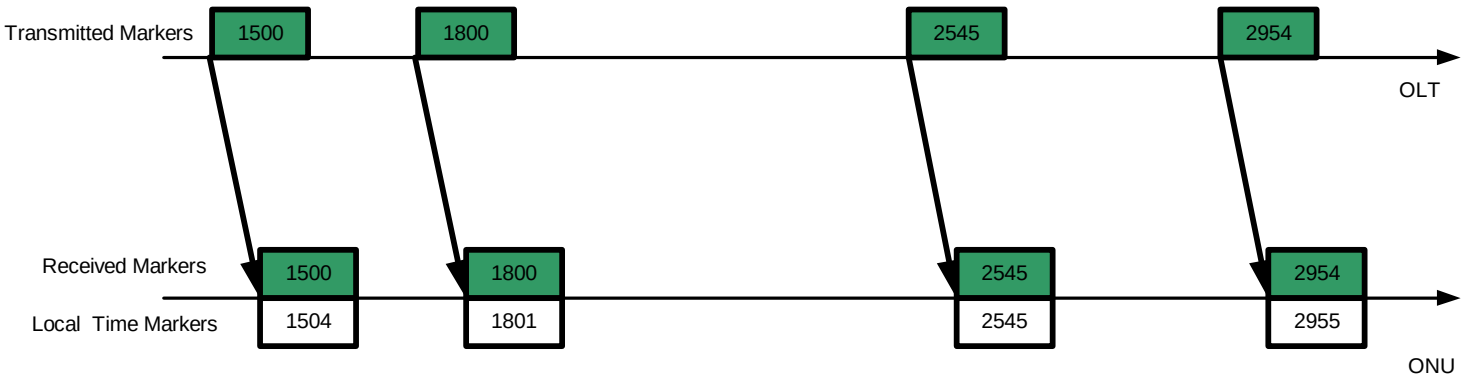
Synchronous Clock Domain



- **The complete system is locked to OLT transmit clock**
- **Needs little guard-band**

Timing Proposal

Timing Operation

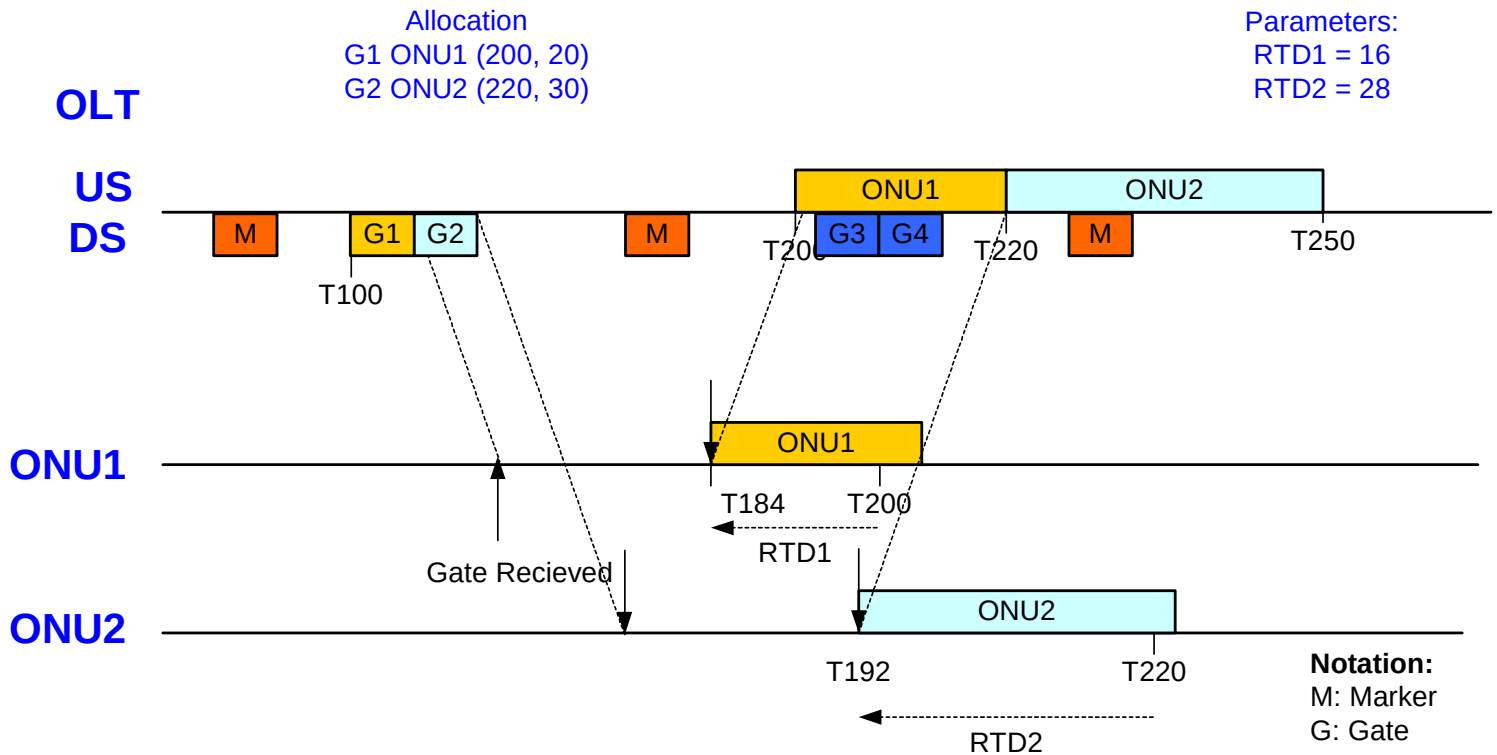


- **OLT frequently transmits a marker (time reference)**
  - Marker contains the timestamp of when this message left the OLT based on a local OLT clock
- **ONU adjusts its local clock to the marker**
  - ONU can update the counter with the received timestamp

Timing Operation (2)

- **The markers are sent frequently**
  - The time between two markers need not be constant
- **Gate messages are transmitted independent of markers**
  - Gate message contains the start time according to clock established by the markers

Timing and Gate Operation



- **Timing operation is independent of Gate operation**

Timing – Pros/Cons

- **Pros**
  - MAC Control operation is independent of Phy layer clocks
  - Simplifies system operation
    - Simplifies the OLT operation
      - It decouples the gate transmission and timing
      - Gate msgs pass through the MAC control without modifications
      - Gate msgs can reach the ONU much ahead of transmission time allowing software implementation
    - Adds one additional register in ONU
  - Keeps the gate allocation mechanism independent of the protocol operation

- **Cons**
  - Markers must be sent periodically
  - Generates a Marker frame in real time

Summary

- **Three clock domain models presented**
  - Asynchronous clock domain
  - Downstream clock domain
  - Independent clock domain
- **It is possible to get the similar timing accuracy with all three models**
- **The proposed timing approach simplifies the overall system operation**

Clock Domain

- **System performance increases marginally from Asynchronous- to Synchronous-clock domains**
- **System cost increases from Asynchronous- to Synchronous-clock domains**