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Full Duplex MII/MAC Interface for VDSL Links

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Outline

- **Introduction and problem statement.**
- **VDSL data throughput adaptation, including HDLC encapsulation requirements.**
- **Clocks/Collision and STA/PTM-TC management.**
- **Possible EoVDSL adaptation layer requirements.**

Introduction

- **The need to adapt the data throughput of the MII/MAC interface to that of the VDSL link.**
- **Main issues:**
  - *MII-MAC rate is 100/10 Mbps. The VDSL data rate is provisioned to something less than 52 Mbps.*
  - *The data throughput mismatch. An active VDSL link requires a consistent rate of payload data. This arises the need for encapsulation and flow control.*

Throughput Adaptation Problemns

- **An auxiliary data FIFO is needed to support the MII in the PTM-TC layer.**
- **Due to FIFO size limitations:**
  - *During idle MAC/MII link, the PTM-TC layer might run out of payload data to support an active VDSL-link.*
  - *It is difficult to control the FIFOs at 100 Mbps MAC/MII over a slower VDSL link.*

Proposed Solutions

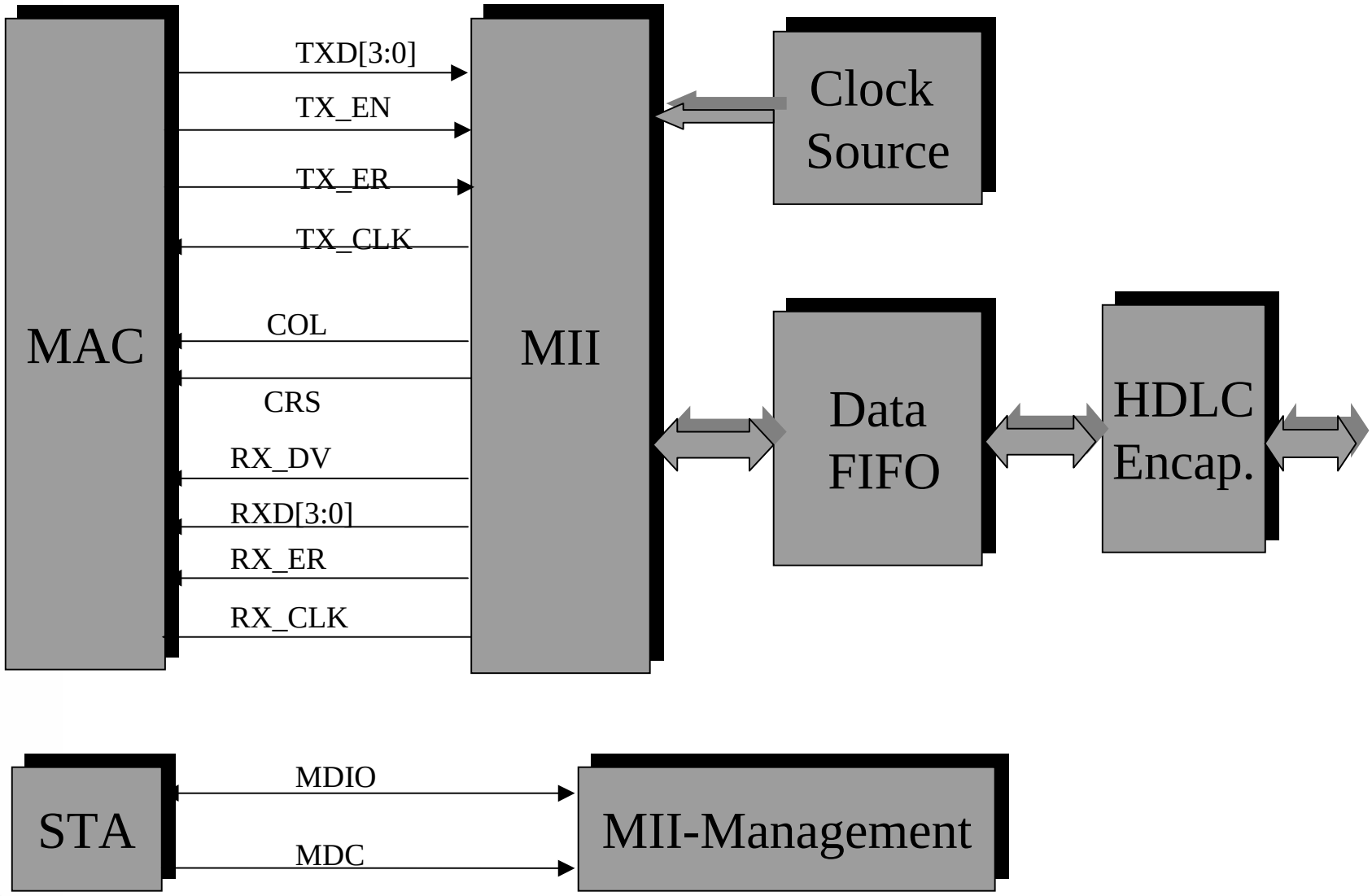
- **The ITU G.993.1 requires HDLC-encapsulation in the PTM-TC layer.**
- **Besides the known HDLC-framing procedure, intra-frame idle byte insertion will provide more freedom in data FIFO control.**
- **After the VDSL-link initialization, the PTM-TC layer sets the proper MII-clock speed (less than 100 Mbps), which controls the data-rate.**

Proposed Solutions

- **Even thought the VDSL link is running full duplex, we can fake a collision between the MII and the MAC to slow down the Tx data rate.**

Clocks and Management

- **The TX_CLK/RX_CLK clock frequency can be controlled by the PTM-TC layer.**
- **Through dedicated MII-management registers, the speed can always be renegotiated between the Station management and the PTM-TC layer.**
- **In critical mismanagement conditions, the PTM-TC layer may stop the TX_CLK/RX_CLK!**



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Possible EoVDSL Adaptation Layer Requirements

- **TX_Clk/RX_CLK Stopping.**
- **Variable data rates, which are less than 100 Mbps.**
- **HDLC-encapsulation with intra-frame idle byte insertion.**
- **Dedicated management registers for passing the suitable clock speed.**