IEEE P802.3ae MDC/MDIO

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Presentation purpose

• Explain what the MDIO interface is
  – For those not familiar with 802.3
• Explain what we have changed and added to the MDIO interface in 802.3ae
  – For those who are familiar with 802.3 but have not been participating in 802.3ae
• Explain how MDIO fits with 802.3ae link status and fault reporting
What is MDIO for?

‘..a simple, two-wire, serial interface to connect a management entity and a managed PHY for the purposes of controlling the PHY and gathering status from the PHY.’

(Clause 22.2.4)
MDIO signals

- MDC (Management Data Clock) sourced continuously from STA (station management entity)
- MDIO (Management Data Input/Output) bi-directional multi-drop bus
Clause 22 MDIO: Up to 32 PHYs

- STA
- MAC 1
- MDI Port 1
- PHY
- MDIO
- MDC
- MAC 32
- MDI Port 32

Up to 32 registers (16 bit) per PHY
Clause 22 MDIO

• PHY status and control
  – Link status
  – Speed ability and selection
  – Power down for low power consumption
  – Duplex mode (full / half)
  – Control of auto-negotiation
  – Fault signalling
  – Loopback

• 2.5MHz MDC speed
  – 39 000 registers per second
# MDIO frame format

<table>
<thead>
<tr>
<th>ST</th>
<th>OP</th>
<th>PHYADR</th>
<th>REGADR</th>
<th>TA</th>
<th>DATA</th>
</tr>
</thead>
<tbody>
<tr>
<td>01</td>
<td>01</td>
<td>Read</td>
<td>5 bits</td>
<td>2</td>
<td>16 bits</td>
</tr>
<tr>
<td>01</td>
<td>10</td>
<td>Write</td>
<td>5 bits</td>
<td>2</td>
<td>16 bits</td>
</tr>
</tbody>
</table>

- ST = 01
- 5 bits
- 5 bits
- 2 bits
- 16 bits

Driven by STA for write, Driven by PHY for read
Issues with Clause 22 MDIO

• Not enough registers for future use
  – Only 4 left unallocated
• Electrical interface requires 5V tolerance
• Does not cater for multi-device PHYs
10GbE adopted proposal

- Use spare ST (start of frame) code (00)
  - Define new indirect addressing register access
  - Applicable to ST code 00 only
  - Access consists of a Address cycle followed by a Read or Write cycle

- Provides many more registers
  - 32 ports as at present
  - 32 MMDs per port (MDIO Manageable Device)
  - 65 536 registers per device
### 10GbE indirect addressing

<table>
<thead>
<tr>
<th>ST</th>
<th>OP</th>
<th>PHYADR</th>
<th>DEVTYPE</th>
<th>TA</th>
<th>ADDRESS/DATA</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**ST = 00**

<table>
<thead>
<tr>
<th>OP</th>
<th>Access Type</th>
<th>Value</th>
<th>Device</th>
</tr>
</thead>
<tbody>
<tr>
<td>00</td>
<td>Address</td>
<td>00000</td>
<td>Reserved</td>
</tr>
<tr>
<td>01</td>
<td>Write</td>
<td>00001</td>
<td>PMD/PMA</td>
</tr>
<tr>
<td>11</td>
<td>Read</td>
<td>00100</td>
<td>PCS</td>
</tr>
<tr>
<td>10</td>
<td>Post Read Inc Addr</td>
<td>00101</td>
<td>PHY XS</td>
</tr>
</tbody>
</table>

**Contents**

<table>
<thead>
<tr>
<th>Access Type</th>
<th>Contents</th>
</tr>
</thead>
<tbody>
<tr>
<td>Address</td>
<td>Address</td>
</tr>
<tr>
<td>Write</td>
<td>Write Data</td>
</tr>
<tr>
<td>Read</td>
<td>Read Data</td>
</tr>
<tr>
<td>Read Inc</td>
<td>Read Data</td>
</tr>
</tbody>
</table>
10GbE indirect addressing example

<table>
<thead>
<tr>
<th>ST</th>
<th>OP</th>
<th>PHYADR</th>
<th>DTYPE</th>
<th>TA</th>
<th>ADDRESS</th>
</tr>
</thead>
<tbody>
<tr>
<td>00</td>
<td>00</td>
<td>0 0000</td>
<td>0 0001</td>
<td>0000</td>
<td>0100 1001 0001</td>
</tr>
</tbody>
</table>

OP = Address
Device Type = PMD
Address to be accessed

<table>
<thead>
<tr>
<th>ST</th>
<th>OP</th>
<th>PHYADR</th>
<th>DTYPE</th>
<th>TA</th>
<th>DATA</th>
</tr>
</thead>
<tbody>
<tr>
<td>00</td>
<td>11</td>
<td>0 0000</td>
<td>0 0001</td>
<td>0000</td>
<td>0100 1001 0001</td>
</tr>
</tbody>
</table>

OP = Read
Device Type = PMD
Data returned
10GbE MDIO devices

Up to 65,536 registers per device
What can the registers do?

- All status and control
  - Link status, speed, power down, fault, loopback
  - PMD capabilities (wavelength, loopback)
  - WIS registers
  - PCS error counters, test patterns
  - XGXS status and control (XAUI)
Fault signalling and link status

- Logic in the previously logic-free RS
- Only the RS can generate RF codes
- Other devices in the link can generate LF codes and must propagate LF codes or RF codes
  - A LF condition overrides a received RF code
- An RS that receives an LF code generates an RF code on the transmit path
- An RS that receives an RF code generates IDLE on the transmit path
Fault signalling and link status

• MDIO used to interrogate devices when an RF code or LF code is received by the RS
  – Check transmit path for a received RF
  – Check receive path for a received LF
• Can only interrogate local devices!
  – Transmission of RF code will trigger a far end interrogation
• Link status can also be checked on a device-by-device basis
Fault signalling example

Remote Fault

Local Fault

PCS fault on receive path

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Fault signalling example

- Local Fault
- Remote Fault
- PCS fault on transmit path
10GbE loopbacks

- XGMII
- XAUI
- DTE XS
- PHY XS
- PCS
- PMA
- PMD

Mandatory
Optional
Mandatory for 10GBASE-R
Not present for 10GBASE-X
Optional for 10GBASE-R
Mandatory for 10GBASE-X
10GbE electrical specification

- $V_{DD} = 1.2V$ typical
- Possible to use open drain drivers

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Minimum</th>
<th>Maximum</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_I$</td>
<td>-0.3V</td>
<td>1.5V</td>
</tr>
<tr>
<td>$V_{IH}$</td>
<td>0.84V</td>
<td></td>
</tr>
<tr>
<td>$V_{IL}$</td>
<td></td>
<td>0.36V</td>
</tr>
<tr>
<td>$V_{OH}$</td>
<td>1.0V</td>
<td>1.5V</td>
</tr>
<tr>
<td>$V_{OL}$</td>
<td>-0.3V</td>
<td>0.2V</td>
</tr>
<tr>
<td>$I_O$</td>
<td>4mA</td>
<td></td>
</tr>
</tbody>
</table>
10GbE MDIO

• Backwards compatibility
  – Possible to integrate a Clause 22 PHY into a Clause 45 MMD and use the new electrical interface with the old frame format

• Optional
  – Not mandatory to implement MDIO – could provide access to registers using another interface
Summary

• New Indirect Address register access defined for 10GbE
• Opens up many more registers
  – 32 Ports
  – 32 MMDs per port
  – 65 536 Registers per MMD
• End-to-end fault signalling
  – Detailed diagnosis via register accesses
• Multiple loopback points defined
• New low voltage electrical specification