Ultra-Fast Burst Mode Clock/Data Recovery (CDR)

Al Dunlop	**Lucent**
Glenn Boles	**Lucent**
Bob Gaglianello	**Lucent**
Manyalibo Matthews	**Lucent**
Dusan Suvakovic	**Lucent**
Dora van Veen	**Lucent**

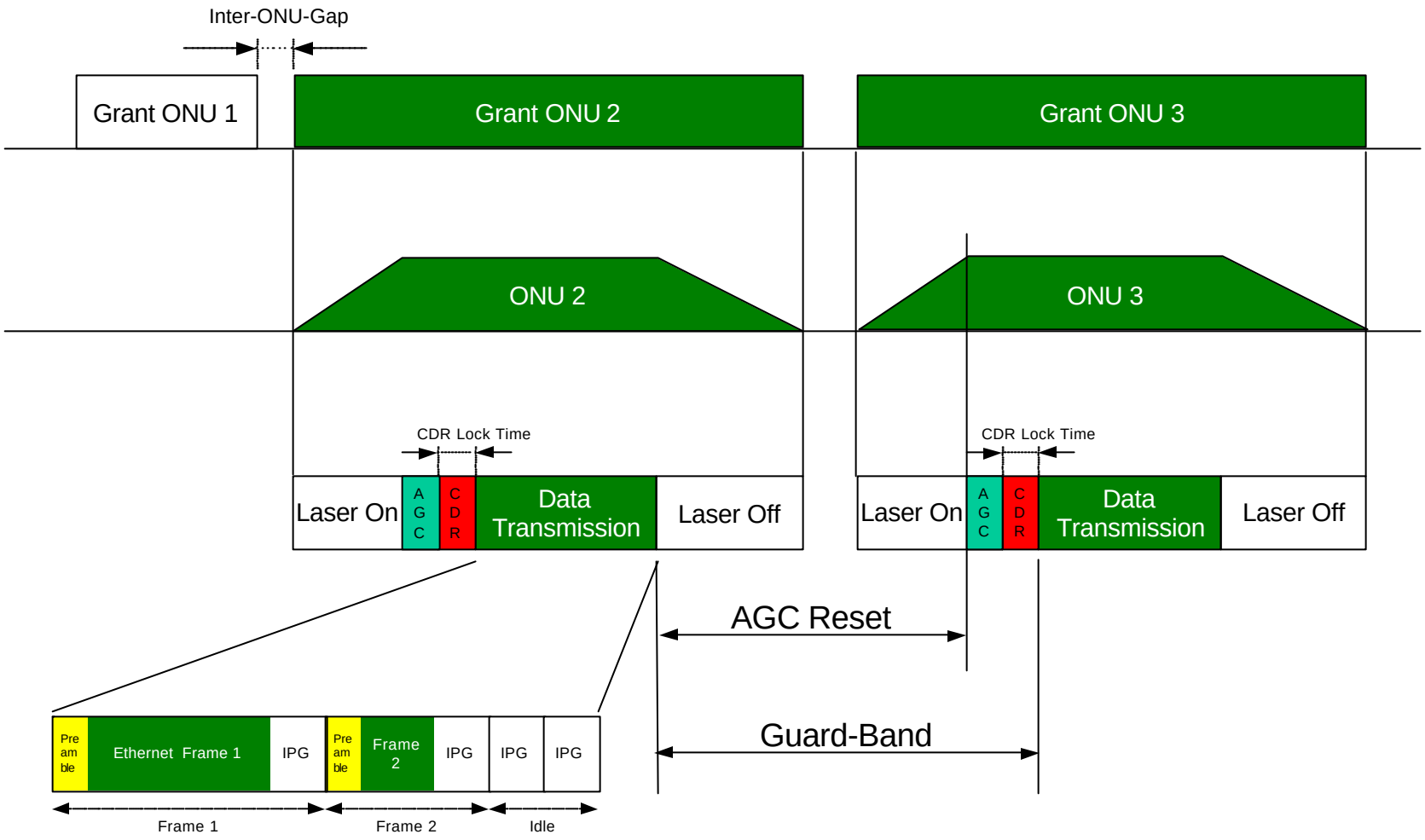
Why do we care about CDR lock times ?

- **The guard band has a significant impact on link efficiency**
  - **Succeeding slides will quantify this**
- **CDR lock time is an important component of the Guard Band (Maislos_optics_1_0702.pdf)**
- **From Bhatt (e-mail correspondence 8/23/2002) sync time for legacy devices: ~1000 bits / transitions**
- **In this presentation we will describe a technique that can sync in a SINGLE transition**

Impact on Link Efficiency of Guard Band

- **Assume:**
  - 1 msec “Gate-Report Cycles” (1000 per second)
  - 64 ONU’s
  - 1, 0.5, 0.1 usec Guard-Band times
- **Total time taken up by Guard-Bands is:**
  - 1000 * 64 * 1.0e-6 = 64 msecs ==> 6.4 % overhead
  - 1000 * 64 * 0.5e-6 = 32 msecs ==> 3.2 % overhead
  - 1000 * 64 * 0.1e-6 = 6.4 msecs ==> 0.64 % overhead
- **Smaller is better, but currently available transceiver pairs typically do not meet the 0.1 usec guard-band. It will be possible with future devices.**

Guard-Band Definition for Purposes of this Presentation



Components of Guard Band

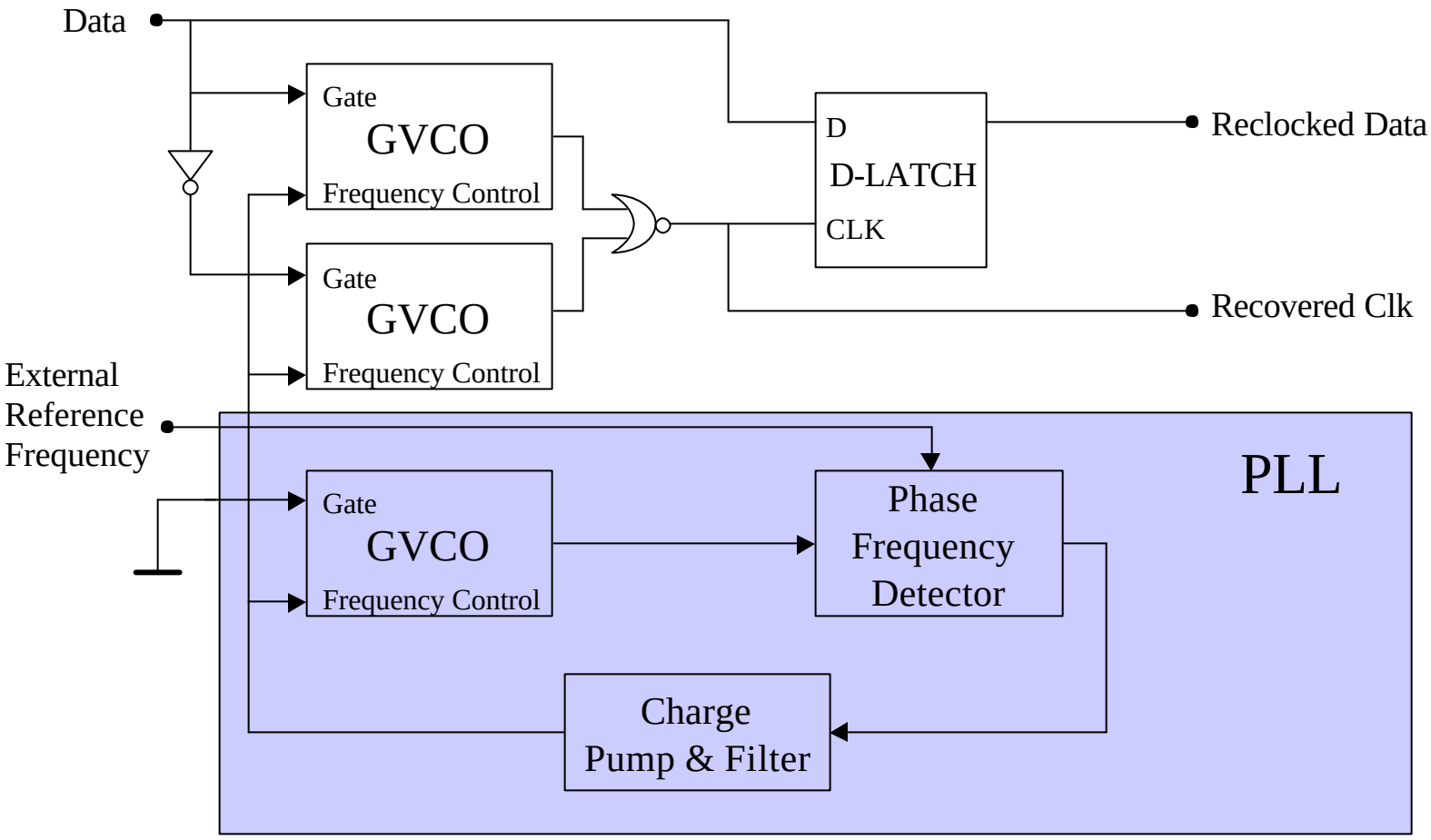
(refer to Maislos_optics_1_0702.pdf)

- **Clock drift allowance + Path change allowance (thermal drift):** 16 nsecs
- **Protocol clock resolution:** 32 nsecs
- **Laser on / Laser off: (**16+16) nsecs for ONU transmitter
- **OLT Receiver AGC delay:** 50 - 100 nsecs
- **CDR Lock time:** 160 - 800 nsecs

  (200 - 1000 bits / transitions)
- **Comma detect:** 48 nsecs

>>> Current CDR lock times dominate <<<

Proposed Burst Mode CDR
(Locks in a Single Transition)



Indirect tuned Gated VCOs

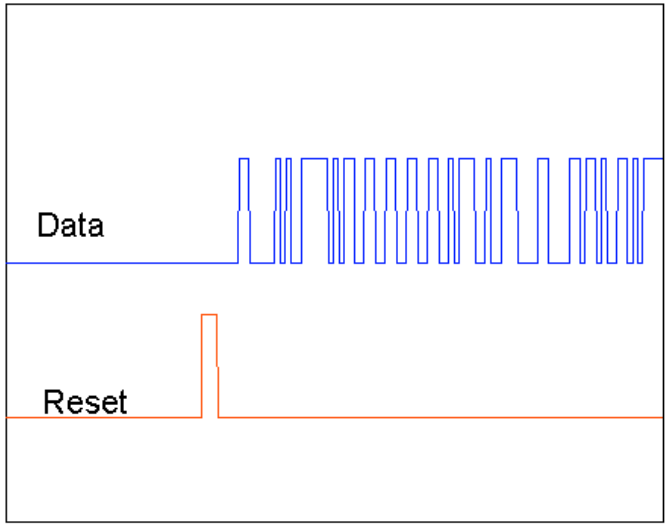
Ref: Y. Ota et al., J. Lightwave Technology, 12(2), 325 (1994)

Non-Overlapping Clock Recovery Methods

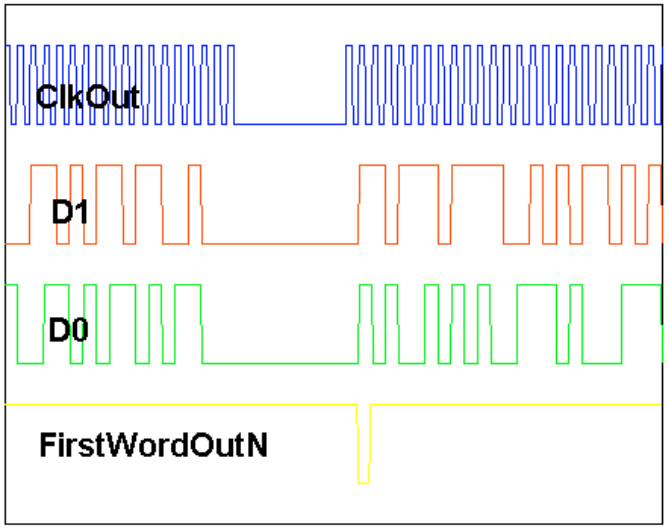
	Narrow-band Systems	Broad-band Systems
Open Loop Approach	e.g., Saw Filter •Simple design, but circuits cannot be fully integrated •"Locking" requires many data transitions (thousands) •Handles only occasional low transition density data patterns •High degree of jitter rejection	Proposed Design •Simple design, fully integrated and small circuit •Locks instantaneously on first data transition •Handles data with low transition density •No jitter rejection
Closed Loop Approach	e.g., narrow-band PLLs •Complex design, circuits difficult to integrate fully •"Locking" requires many data transitions (thousands) •Handles data with low transition density •High degree of jitter rejection	e.g., broad-band PLLs •Design of moderate complexity, circuits can be fully integrated •Locking requires at least 5 to 10 transitions •Does not handle easily data with low transition density •Low degree of jitter rejection

Burst Mode (One Bit / Transition) Clock and Data Recovery at 1.25Gb/sec

Input



Output



- Burst Mode Clock Recovery can be done at 1.25Gb/s (in standard digital CMOS process)
- Can be bit aligned based on first data “1” or word recognition
- Data can be retimed to give continuous output clock

Availability of Fast Burst-Mode Clock Recovery Technology

- Agere previously announced the availability of a chip implementing fast burst-mode clock recovery
  - http://www.agere.com/docs/OT01296.pdf
  - Agere part # AGRBS1G25
- Agere now appears to have withdrawn this chip from the market
- Due to the separation of Agere from Lucent, Bell Labs is now precluded from presenting any actual measurement data from this chip to illustrate the capabilities of the technology

Taking Advantage of Ultra-Fast CDR: Augment Discovery Messages

- **With this CDR technique, guard band overhead can be drastically reduced.**
- **The Discovery Protocol should enable the efficient use of either current PMD's and future high-performance PMD's.**
- **In order to efficiently support both, the Discovery Protocol Messages should include the following parameters:**
  - **Toff, Ton, Tagc, Tcdr**