IEEE 802.3ah EFM

OLT Clock and Data Recovery Re-lock Time Report

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1000BASE-X Re-lock Time Report

- In Vancouver the following actions were taken:
  - *Determine what the re-lock times were in present 1000BASE-X Serializer / De-serializer products today.*
  - *Determine what the re-lock times could be made to achieve without significant architectural change.*

Definition of Re-lock Time

- Not all 1000Base-X SERDES in the market specify a minimum "Re-lock Time." Interpretations of re-lock when discussed varied.
- To help discussion the following definition of re-lock was made:
  - *The minimum time from a point of stable data recovery with BER of 10^{-12} to the same point* when the incoming data stream is phase shifted 90 degrees. The incoming data is assumed to meet the 1000Base-X Far end eye template.*

** As measured by assertion of comma detect.*

1000BASE-X Re-lock Times

- There are two general types of 1000BASE-X Clock and Data Recovery (CDR) architectures in the market today:
  - Phase Lock Loop (PLL) - PLL based CDR's react to a change is the edge position of received data by adjusting analog parameters (such as charge pump current).
    - Available in CMOS on discrete solutions both single and multiple port products.
  - Digital Sampler - Digital Sampler based CDR's react to a change in the edge position of received data by collecting enough edge positions to meet the decision criteria, then moving the sample point in the direction of the edge.
    - Available in CMOS in both discrete solutions and ASIC libraries.

1000BASE-X Re-lock Times

Determine what the re-lock times were in present 1000BASE-X Serializer / De-serializer products today:

- PLL based CDR's - Response time for a worst case phase shift is typically 125 bits (100ns) or less.
  - This has been measured in the lab.

- Digital Sampler based CDR's - Response time for a worst case phase shift is typically 1000 bits (800ns).
  - This has also been measured in the lab.

Possible 1000BASE-X Re-lock Times

Digital Sampler re-lock times can be reduced. Three possible options:

1. Reduce the number of edge samples taken before a decision is made.
   - Increases sensitivity to data dependent jitter.
2. Increase the phase step for a given decision.
   - Increases sensitivity to hunting jitter.
3. Selectable phase steps chosen by a modified decision algorithm.
   - Basically, the further away, the bigger the step.
   - *This option is not a significant change to existing digital sampler architectures.*

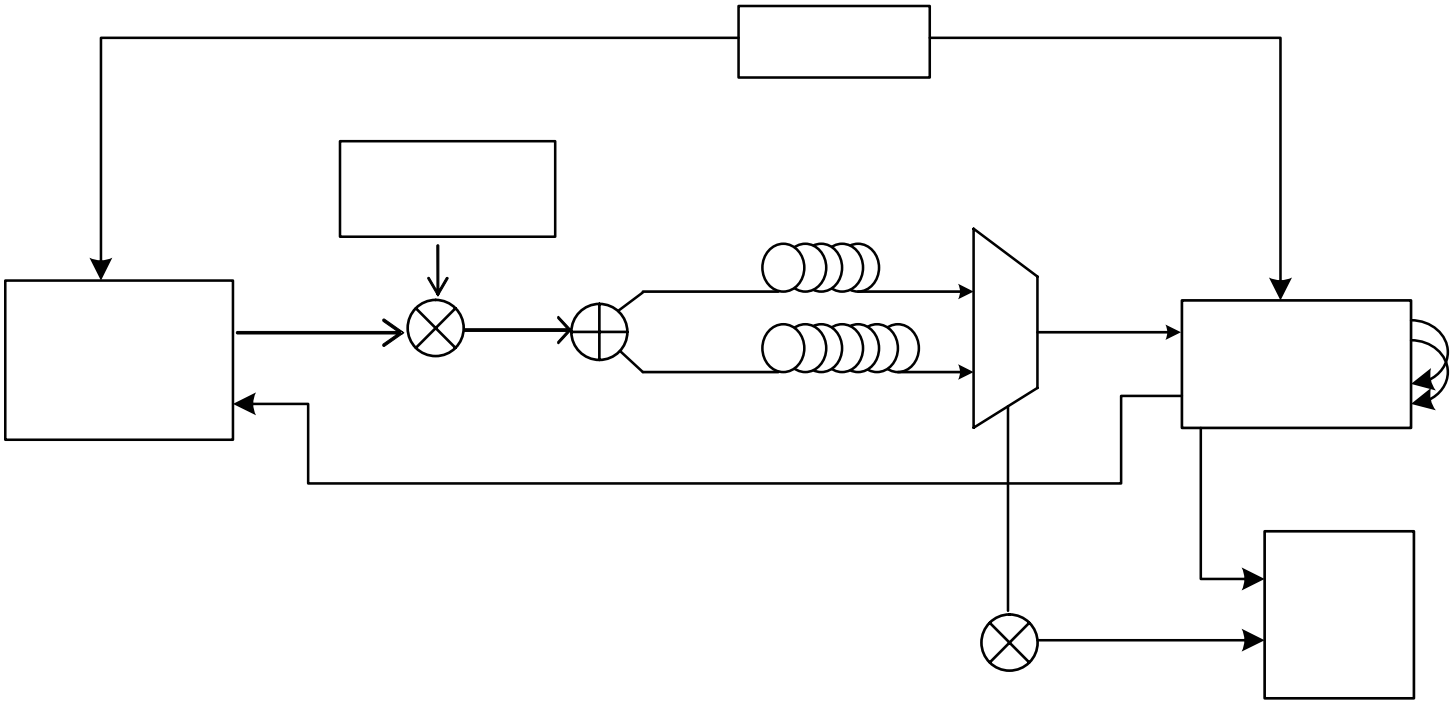
Possible 1000BASE-X Re-lock Times

Determine what the re-lock times could be made to achieve without significant architectural change.

- Using the proposed solution, digital sampler based CDR re-lock times can be reduced to 625 bits (500ns) without significant change to existing architectures.

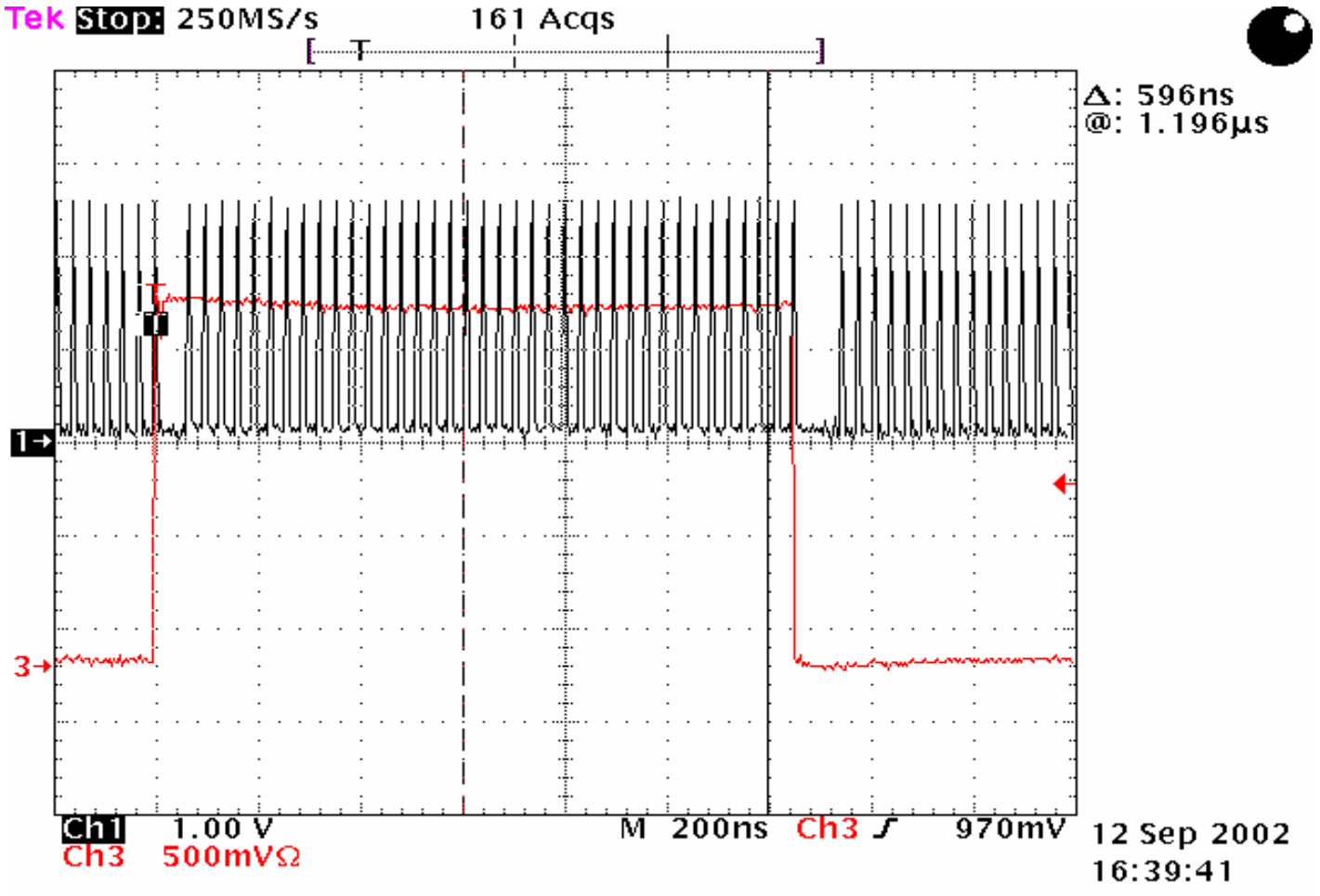
Additional Data

Test Method for Re-lock



- Data pattern used was K28.5, D5.6
- Re-lock was measured from the rising edge of Toggle Clock to the rising edge of Comma Detect

Example Re-lock Test Results



Summary

- Existing 1000BASE-X CDR's have re-lock times between 100ns (PLL) to 800ns(DLL).
- Digital Sampler based CDR re-lock response times can be improved to 500ns without signification change.
- Faster re-lock times will require an alternate CDR architectures.