**101.3.2.4 FEC encoding process**

The {EPoC\_PMD\_Name} encodes the transmitted data using Low-Density Parity-Check (LDPC) (FC, FP) code. The CLT {EPoC\_PMD\_Name} PCS operating on active CCDN shall encode the transmitted data using one of the LDPC (FC, FP) codes per Table 101-1, as selected using register TBD. The CNU {EPoC\_PMD\_Name} PCS operating on active CCDN shall encode the transmitted data using one of the LDPC (FC, FP) codes per Table 101-2, as selected using register TBD.

Annex 101A gives an example of LDPC (FC, FP) FEC encoding. {we will need to select one of the codes from the family of codes we use in either downstream or upstream and then generate examples}

TABLE101-1: LDCP codes used by the CLT {EPoC\_PMD\_Name} PCS for active CCDN

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Codeword size FC [bits] | Parity size FP [bits] | Code rate R | Number of 65-bit blocks Q | Padding bits W |
| 16200 | 1800 | 8/9 | 221 | 35 |

{content of this table was taken from the approved baseline: [prodan\_3bn\_01a\_0713.pdf](http://www.ieee802.org/3/bn/public/jul13/prodan_3bn_01a_0713.pdf), separated into upstream and downstream directions}

TABLE 101-2 LDCP codes used by the CNU {EPoC\_PMD\_Name} PCS for active CCDN

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Codeword size FC[bits] | Parity size FP[bits] | Code rate R[ ] | Number of 65-bit blocks Q | Padding bits W |
| 16200 | 1800 | 8/9 | 221 | 35 |
| 5940 | 900 | 28/33 | 77 | 35 |
| 1120 | 280 | 3/4 | 12 | 60 |

{content of this table was taken from the approved baseline: [prodan\_3bn\_01a\_0713.pdf](http://www.ieee802.org/3/bn/public/jul13/prodan_3bn_01a_0713.pdf), separated into upstream and downstream directions; more FEC codes are likely to be }

{note – I assume that the FEC code type for transmit direction is selected statically at device startup, and does not change until the device is reset or re-registered in the case of CNU; if we need dynamic changes in the FEC parameter during the operation, I suggest we examine this approach after we have built the first description of the FEC encoding process}

**101.3.2.4.1 LDPC algorithm**



{this material was taken from the approved baseline: [prodan\_3bn\_01a\_0713.pdf](http://www.ieee802.org/3/bn/public/jul13/prodan_3bn_01a_0713.pdf), and needs further development into a consistent and short (as possible) description – I will be looking for some help here – otherwise, I will only convert what was approved with simple text edits}

**101.3.2.4.2 LDPC encoding process**

The process of padding FEC codewords and appending FEC parity octets in the {EPoC\_PMD\_Name} PCS transmitter is illustrated in Figure 101-1. The 64B/66B encoder produces a stream of 66-bit blocks, which are then delivered to the FEC encoder. The FEC encoder accumulates Q (see Table 101-1 for CLT PCS and Table 101-2 for CNU PCS) of these 66-bit blocks to form the payload of a FEC codeword, removing the redundant first bit (i.e., sync header bit <0>) in each 66-bit block received from the 64B/66B encoder. The first bit <0> of the sync header in the 66-bit block in the transmit direction is guaranteed to be the complement of the second bit <1> of the sync header – see 49.2.4.3 for more details.

Next, the FEC encoder prepends W (see Table 101-1 for CLT PCS and Table 101-2 for CNU PCS) padding bits (binary 0) to the previously aggregated series of 65-bit blocks (blocks C1 through CQ), forming the payload of the FEC codeword as shown in Figure 101-1. This data is then LDPC-encoded, resulting in the (FC-FP)-octet parity portion of the FEC codeword. The (FC-FP)-octet payload portion (blocks PY1 through PYQ) and FP-octet parity portion of the FEC codeword are then combined to form the FC-octet LDPC codeword. The padding bits are used to generate the FEC codeword but are not transmitted across the PMA onto the medium.



FIGURE 101-1: PCS Transmit bit ordering

**101.3.2.4.3 LDPC codeword transmission order**

As shown in Figure 101-1, once the parity for the FEC codeword is calculated, the FEC encoder constructs the transmittable FEC codeword comprising the payload followed by the parity.

The FEC payload comprises the sequence of Q 65-bit blocks generated as discussed in 101.3.2.4.2.

The FEC parity comprises the sequence of FP bits, generated per 101.3.2.4.2, divided into a series of 65-bit blocks.

**101.3.2.4.4 State diagram**

{State Diagrams for FEC will be added once we agree on the operational details, how padding is used and what we are actually aggregating at what time and in what fashion}

**101.3.2.5 Data Detector**

{The presence of the Data Detector remains for discussion at this time, given that EPoC does not use lasers and there was no clear need demonstrated until now for anything like a Data Detector function}