

UPDATE THE PROPOSAL FOR PHY LINK CHANNEL FEC

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- **Robustness: PLC must be received by new CNUs to enable joining the network**
 - CLT may select the channel to run at the best available part of the spectrum
 - Must be very robust to worst case expected channel conditions for the new CNU
 - Worst case SNR a modem can support (on the best available part of the spectrum)
 - Protect against notches in spectrum caused by reflections
 - Plus some margin to protect against spurs
 - Probably will not use frequencies subject to known external interference (LTE..)
- **Protection against burst noise**
 - PLC is not interleaved with data
 - PLC frame is separately spread over multiple symbols
 - Codewords need to be long enough to overcome expected burst durations
 - Codewords over the PLC frame should not be too long to not increase latency too much

■ AWGN

- 256-QAM requires an average SNR of 24 dB with no margin
- Worst case attenuation of a group of eight subcarriers due to SCTE 40 reflections is 4 dB
- Assume some margin for worse loops and/or spurs and/or additional margin taken ~ 4 dB
- **Target SNR of ~ 16 dB to receive the PLC**
- 16-QAM plus FEC with 75% code rate (effective PLC data rate is about 750 kbps with the lowest number of subcarriers)

■ Burst Noise

- Assume worst case burst noise limits of
 - 16 μ s @ 5 dB SNR over two OFDM symbols
 - 10 μ s @ 10 dB SNR over two OFDM symbols
- Two OFDM symbols may be impacted by the burst noise

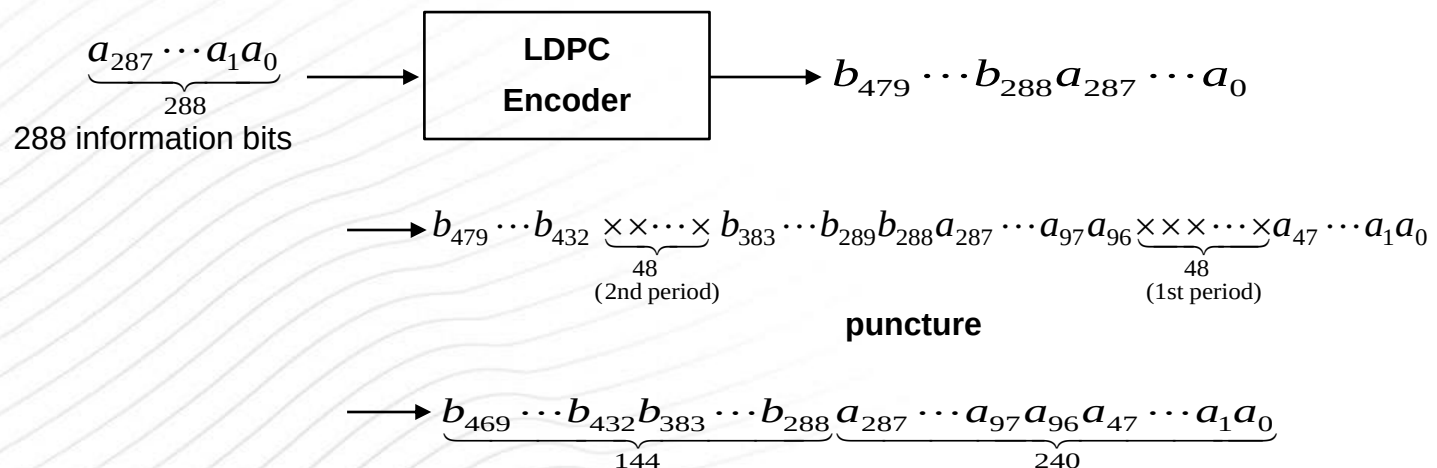
■ 75% (384,288) binary punctured LDPC code

- Mother LDPC code: 60% (480,288) code
 - 4x10 base parity check matrix with sub-matrix size (lifting value) equal 48.
 - Parity check matrix

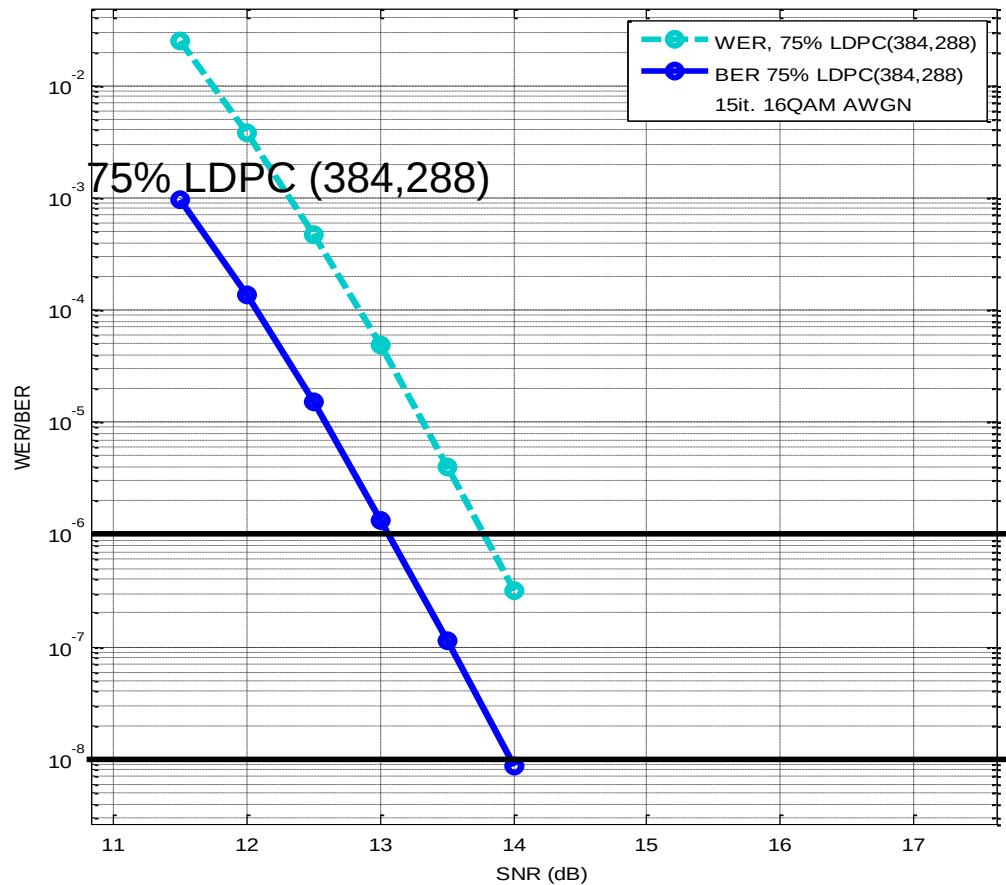
16	1	28	9	40	38	16	-1	-1	-1
28	42	36	11	39	9	8	38	-1	-1
5	2	18	16	25	47	-1	2	19	-1
18	18	40	18	0	34	-1	-1	7	32

- (384, 228) code is obtained by puncturing (480,288) mother code

- Two period puncturing
 - Period 1: size 48 start at 48 (puncturing information bits)
 - period 2: size 48 start at 384 (puncturing parity bits)



PERFORMANCE ON AWGN CHANNEL



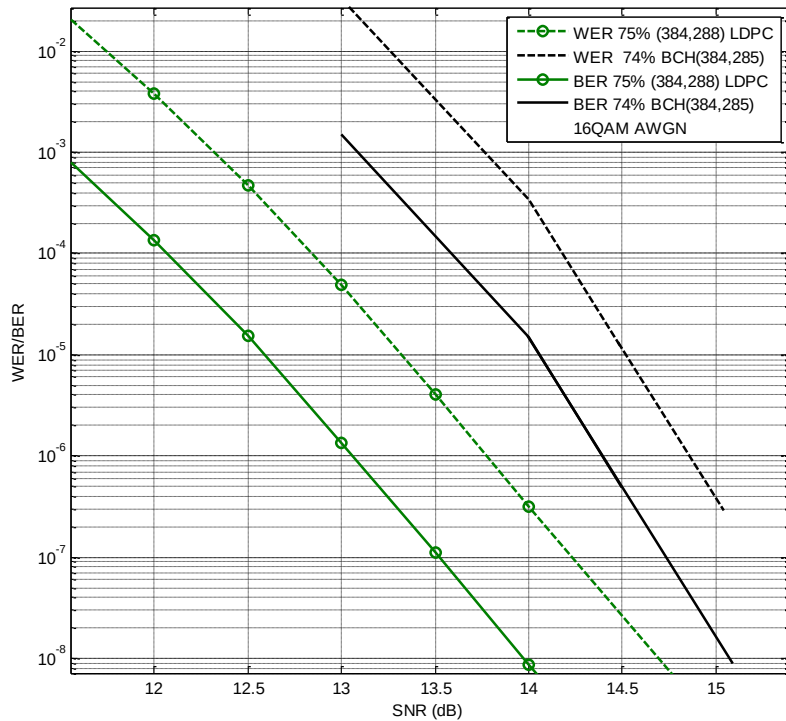
WER=1e-6

13.8dB

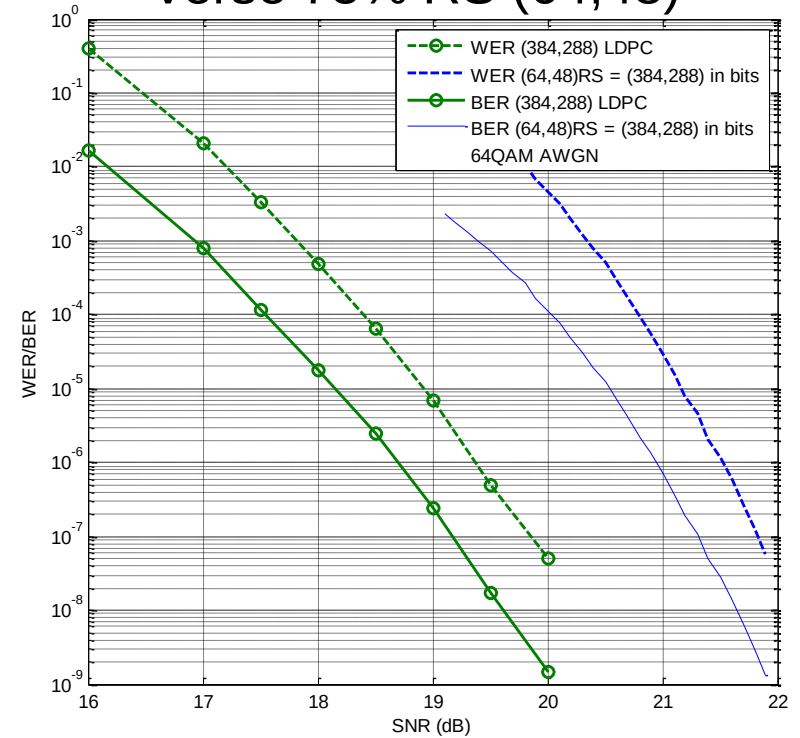
BER=1e-8

14dB

Verse 74% BCH (384,285, t=11)



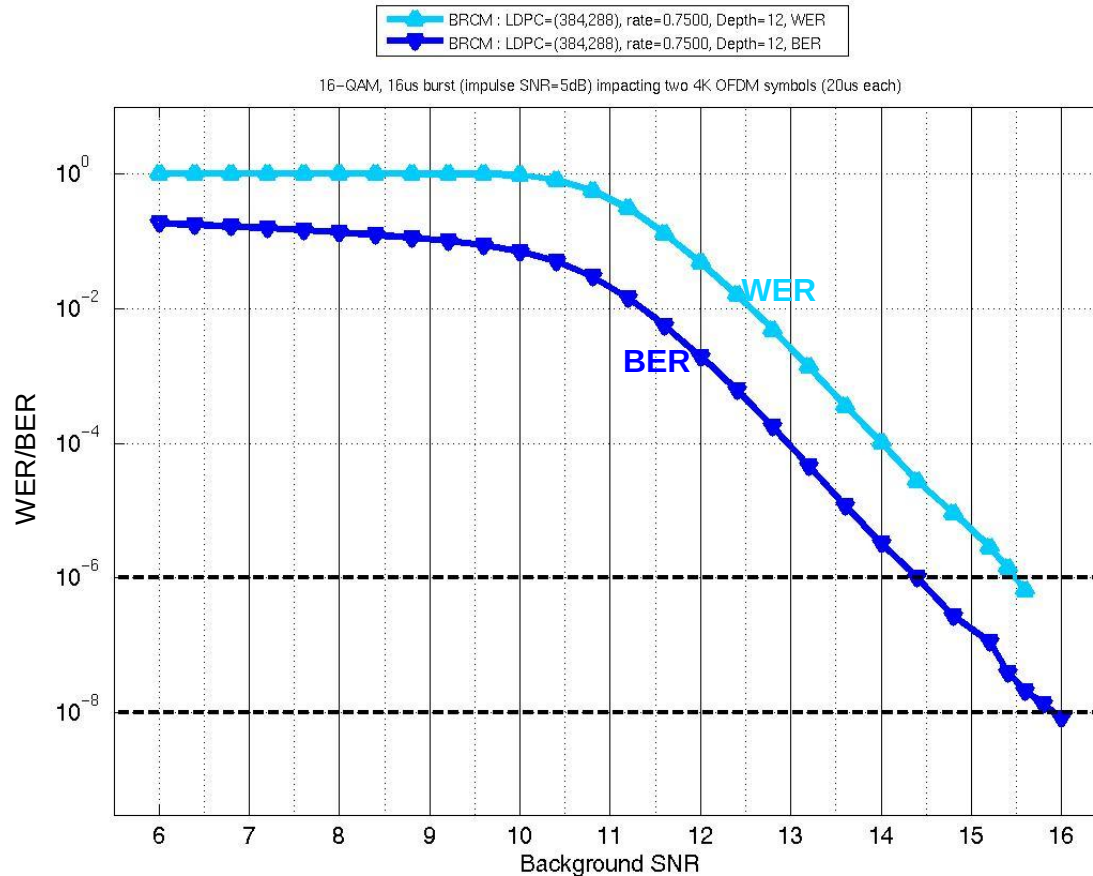
Verse 75% RS (64,48)



PERFORMANCE ON IMPULSE/BURST NOISE

16 μ s BURST WITH 5 dB BURST SNR

12 symbol latency, Impulse noise impacts two 20 μ s symbols



Max. 15 iterations

WER=1e-6

15.5dB

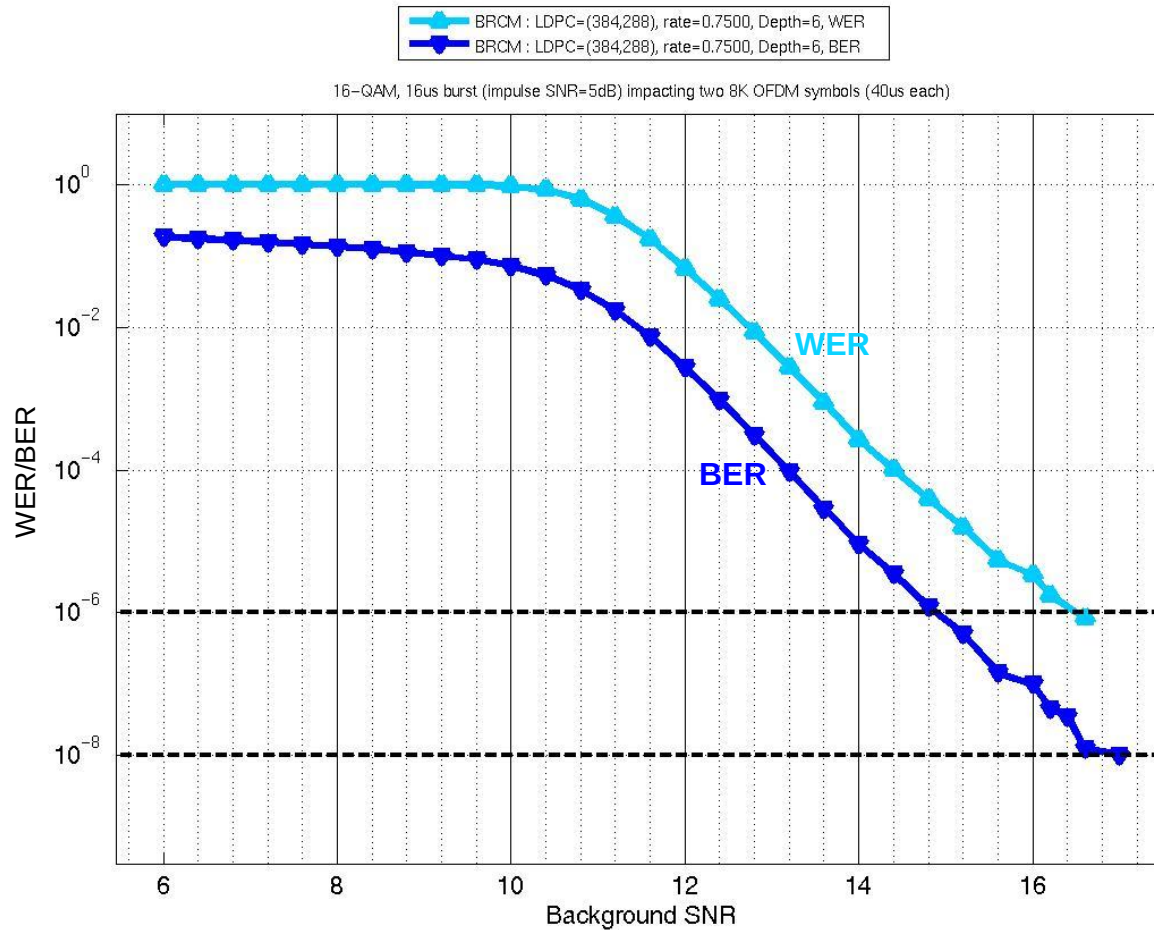
BER=1e-8

15.8dB

PERFORMANCE ON IMPULSE/BURST NOISE

16 μ s BURST WITH 5 dB BURST SNR

6 symbol latency, Impulse noise impacts two 40 μ s symbols



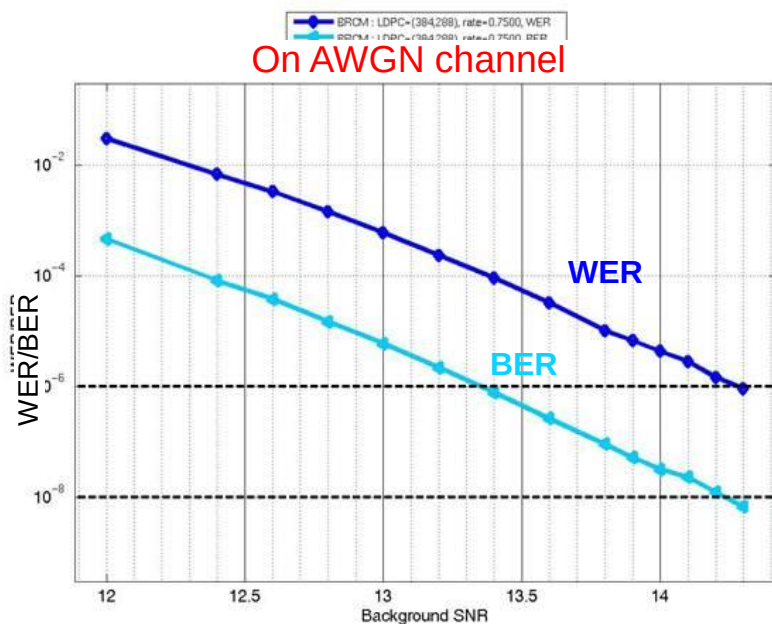
WER=1e-6

16.2 dB

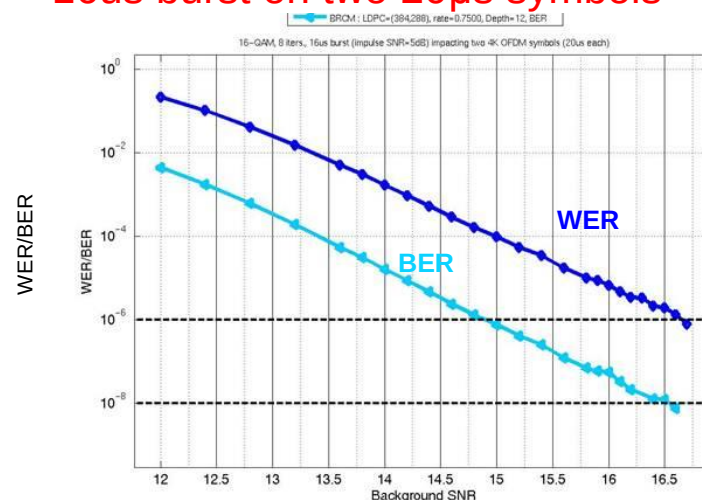
BER=1e-8

16.2 dB

- The figures below show the performance with maximum 8 iterations

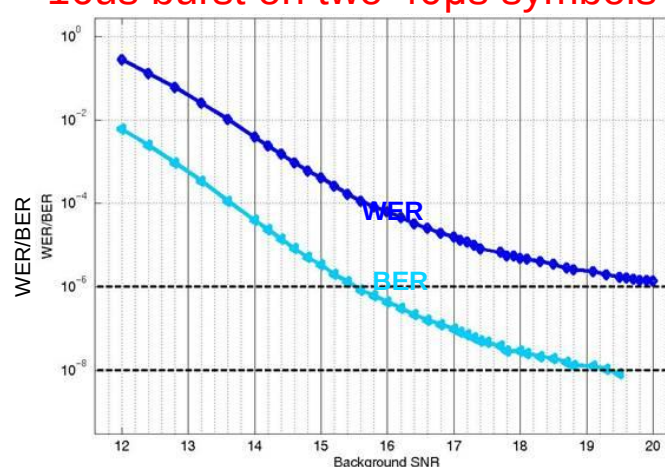


16us burst on two 20μs symbols



- BER < 10^{-8} SNR = 14.5 dB with AWGN
- BER < 10^{-8} SNR = 16.5 dB with burst noise on 20us symbol
- 0.5 dB degradation compared to 15 iterations

16us burst on two 40μs symbols



- **An LDPC code for the PLC is proposed**
 - Code rates: 75%
 - Code latency: 270 uSec
 - SNR = 13 dB to 16 dB with AWGN and Burst noise
 - Complexity negligible (three orders of magnitude lower) compared to the downstream data decoder

- **Do you support to select the LDPC FEC presented at “802.3bn PHY Link Ad Hoc Conference Call June 19 and June 26, 2013” for the PLC FEC**

Thank You