A PROPOSAL FOR PHY LINK CHANNEL FEC

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PLC Considerations

- **Robustness: PLC must be received by new CMs to enable joining the network**
  - CMTS can select the channel to run at the best available part of the spectrum
  - Must be very robust to worst case expected channel conditions for the new CM
  - Worst case SNR a modem can support (on the best available part of the spectrum
  - Protect against notches in spectrum caused by reflections
    - Plus some margin to protect against spurs
  - Probably will not use frequencies subject to known external interference (LTE..)
- **Protection against burst noise**
  - PLC is not interleaved with data
  - PLC frame is separately spread over multiple symbols
  - Codewords need to be long enough to overcome expected burst durations
  - Codewords over the PLC frame should not be too long to not increase latency

FEC Robustness

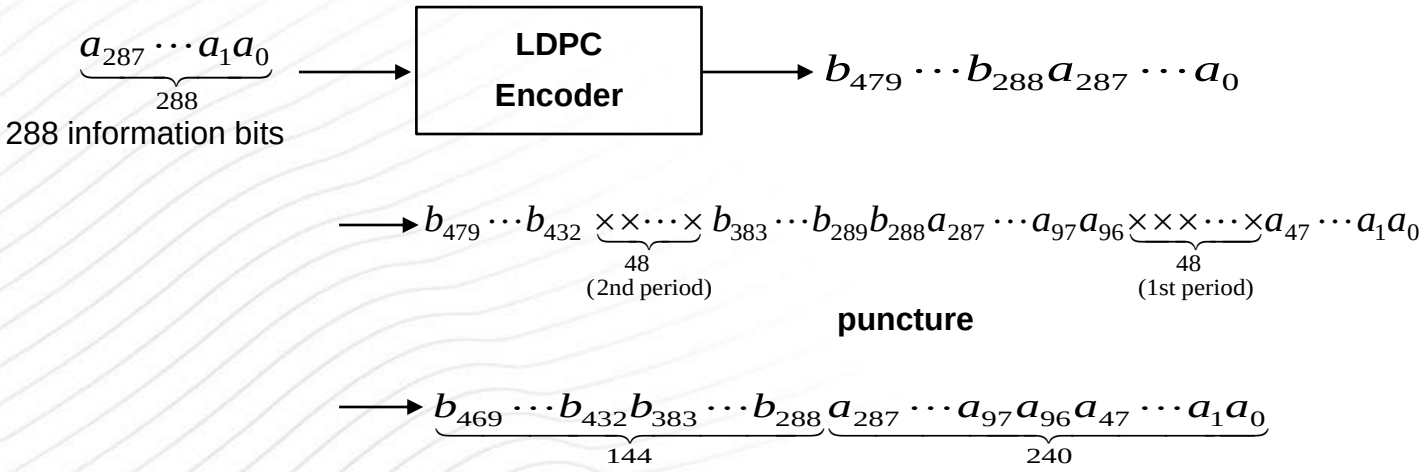
- **AWGN**
  - 256-QAM requires an average SNR of 24 dB with no margin
  - Worst case attenuation of a group of eight subcarriers due to SCTE 40 reflections is 4 dB
  - Assume some margin for worse loops and/or spurs and/or additional margin taken ~ 4 dB
  - **Target SNR of ~ 16 dB to receive the PLC**
  - 16-QAM plus FEC with 50% code rate (effective PLC data rate is about 750 kbps with the lowest number of subcarriers)
- **Burst Noise**
  - Assume worst case burst noise limits of
    - 16 µs @ 5 dB SNR over two OFDM symbols
    - 10 µs @ 10 dB SNR over two OFDM symbols
  - Two OFDM symbols may be impacted by the burst noise

RATE 75% (384,288) LDPC CODE

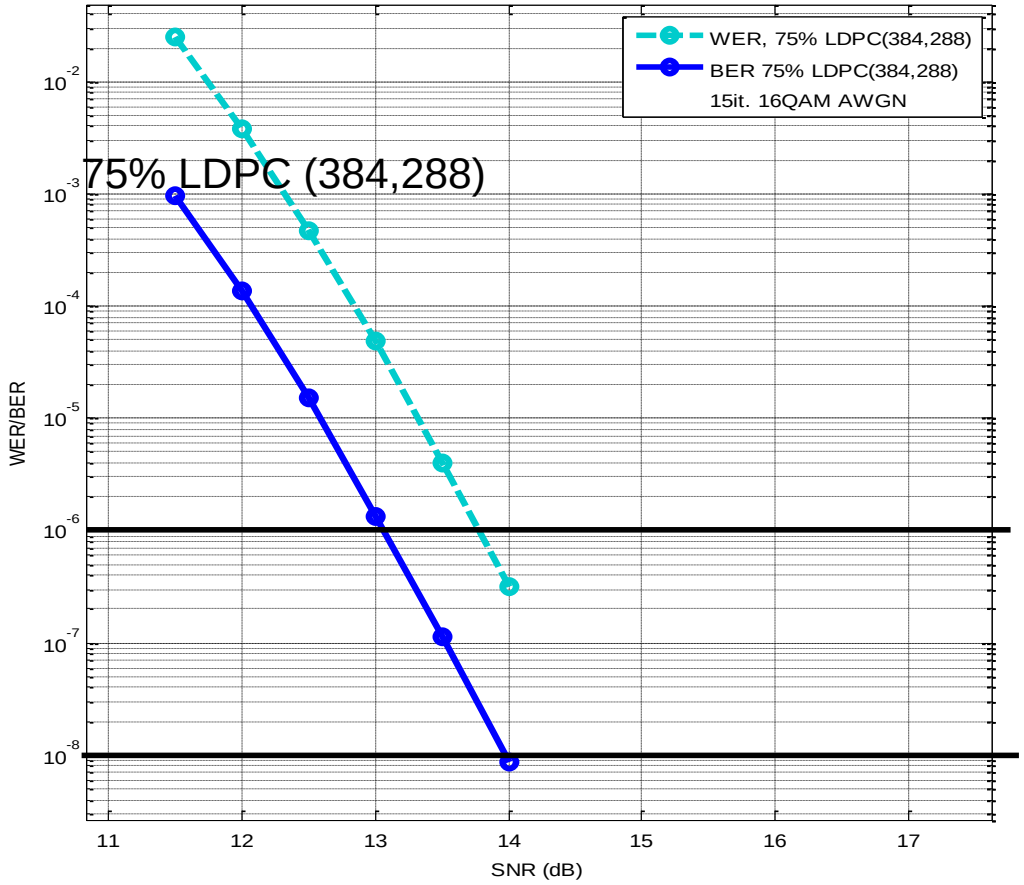
- **75% (384,288) binary shortened and punctured LDPC code**
  - Mother LDPC code: 65% (480,288) code
    - 4x10 base parity check matrix with sub-matrix size (lifting value) equal 48.
    - Parity check matrix

16	1	28	9	40	38	16	-1	-1	-1
28	42	36	11	39	9	8	38	-1	-1
5	2	18	16	25	47	-1	2	19	-1
18	18	40	18	0	34	-1	-1	7	32

  - (384, 228) code is obtained by puncturing (480,288) mother code
    - Two period puncturing
      - Period 1: size 48 start at 48 (puncturing information bits)
      - period 2: size 48 start at 384 (puncturing parity bits)



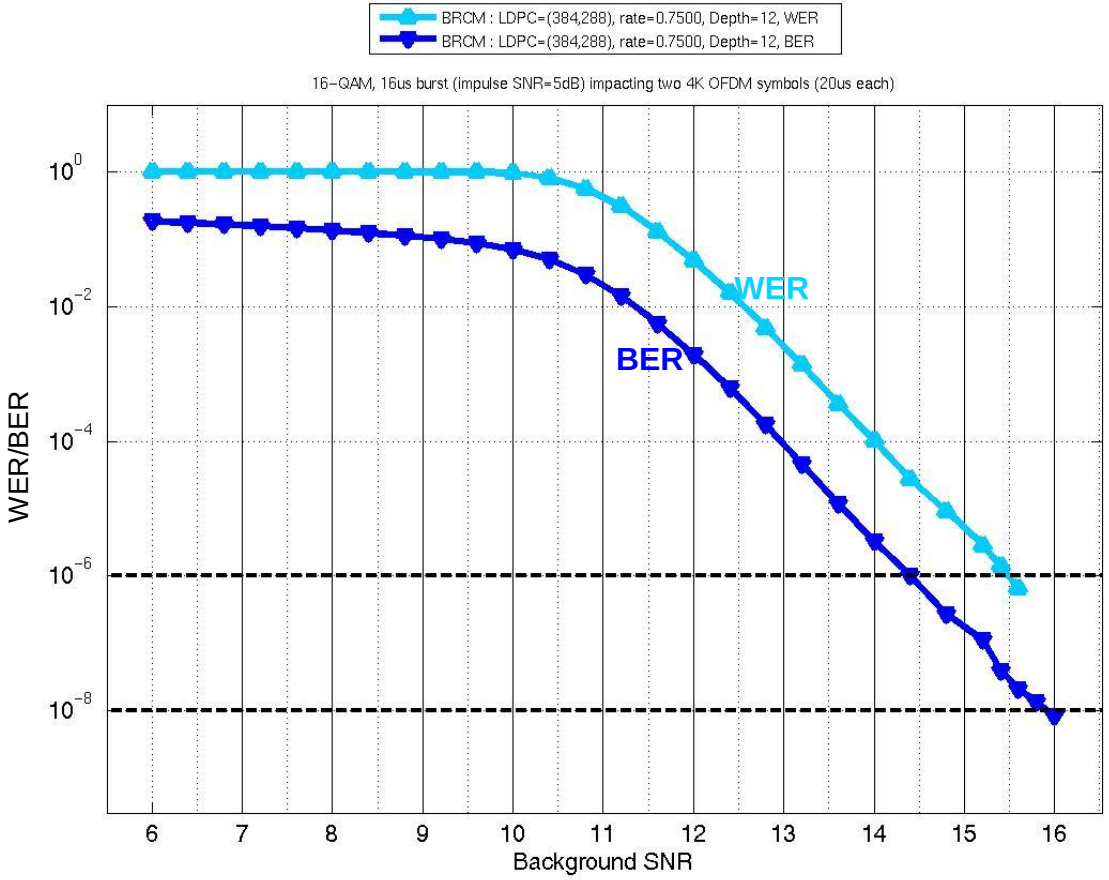
PERFORMANCE ON AWGN CHANNEL



WER=1e-6	BER=1e-8
13.8dB	14dB

PERFORMANCE ON IMPULSE/BURST NOISE
16 µS BURST WITH 5 dB BURST SNR

12 symbol latency, Impulse noise impacts two **20 µs** symbols

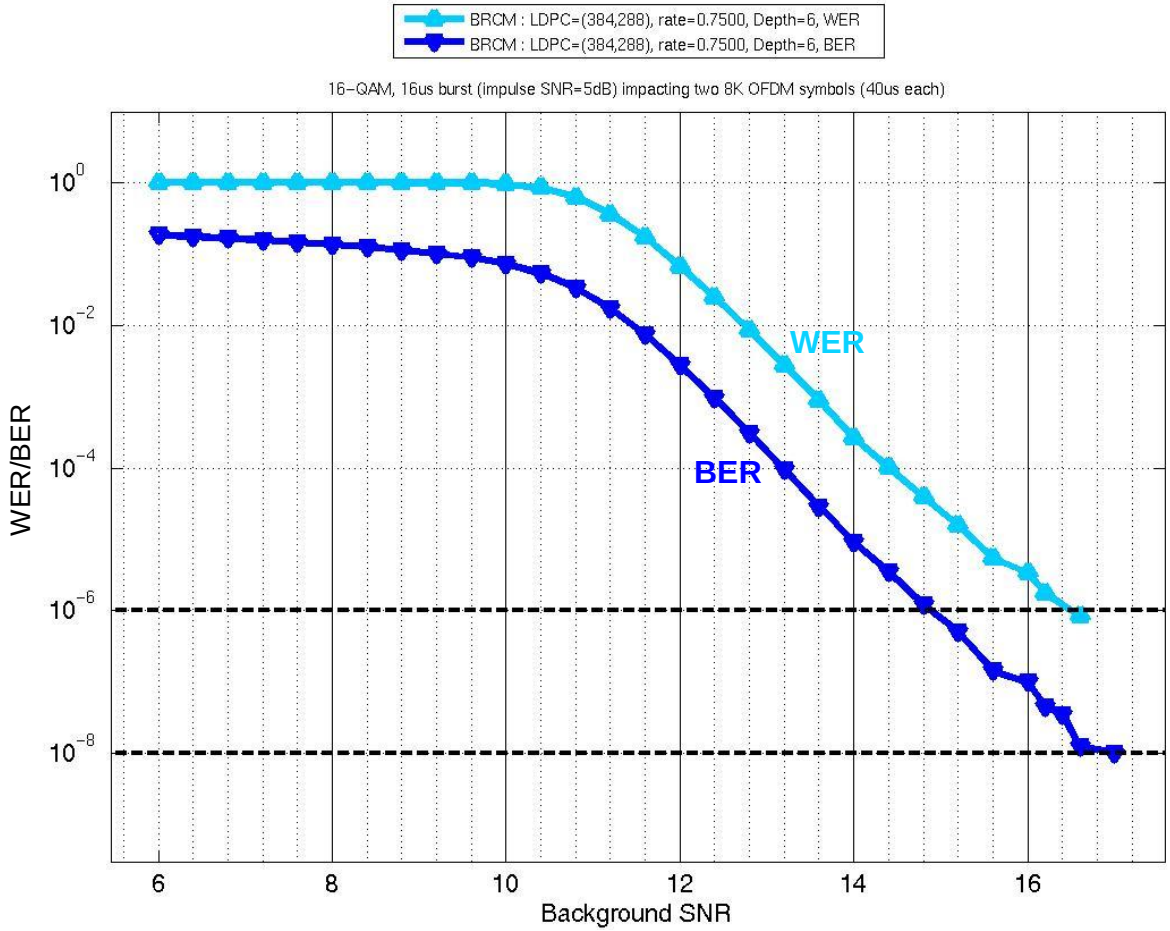


Max. 15 iterations

WER=1e-6	BER=1e-8
15.5dB	15.8dB

PERFORMANCE ON IMPULSE/BURST NOISE
16 µS BURST WITH 5 dB BURST SNR

6 symbol latency, Impulse noise impacts two **40 µs** symbols



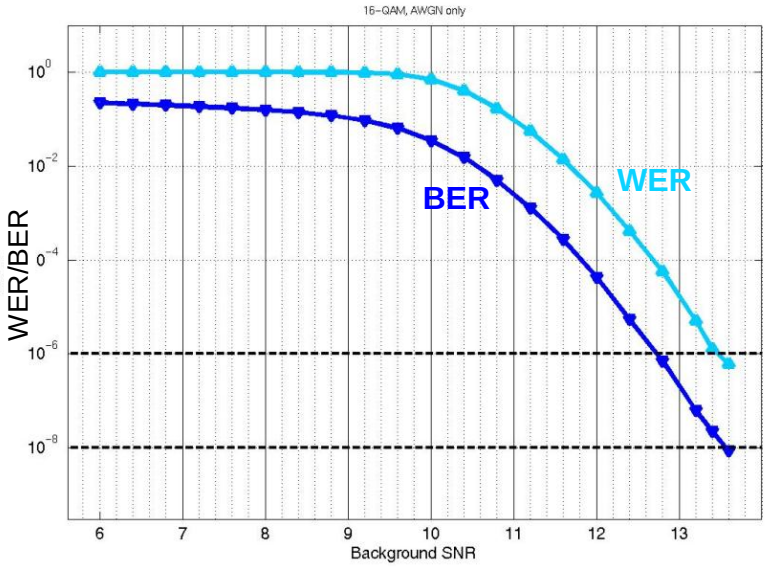
Max. 15 iterations

WER=1e-6	BER=1e-8
16.2 dB	16.2 dB

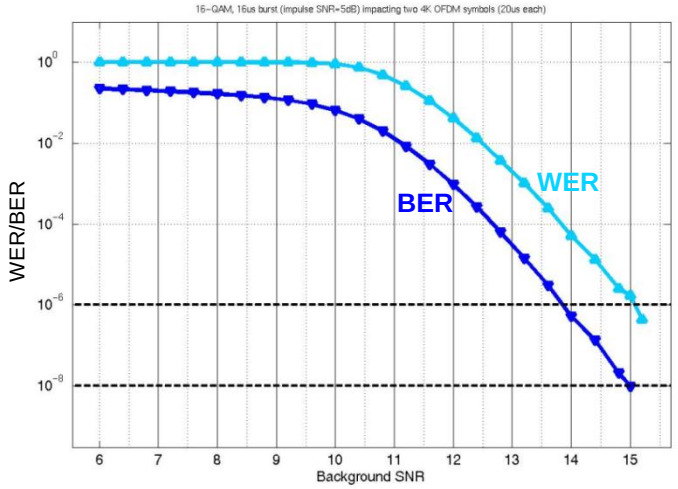
REDUCING NUMBER OF ITERATIONS

- **The figures below show the performance with maximum 8 iterations**

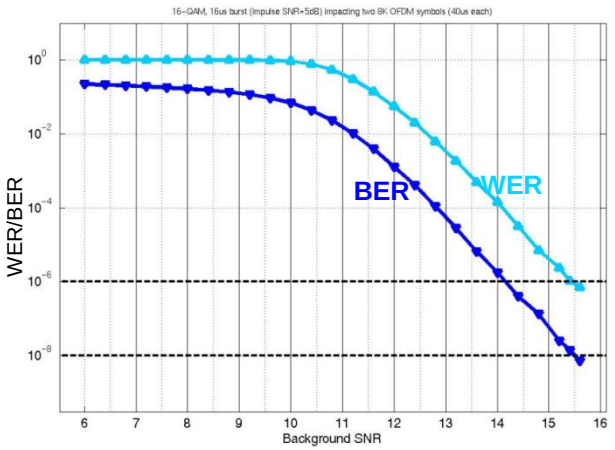
On AWGN channel



16us burst on two 20µs symbols



16us burst on two 40µs symbols



- **BER< 1e-8 SNR = 13.5 dB with AWGN**
- **BER< 1e-8 SNR = 15.5 dB with burst noise**
- **1 dB degradation compared to 15 iterations**

CONCLUSIONS

- **An LDPC code for the PLC is proposed**
  - Code rates: 75%
  - Code latency: 270 uSec
  - SNR = 13 dB to 16 dB with AWGN and Burst noise
  - Complexity negligible (three orders of magnitude lower) compared to the downstream data decoder

Thank You