Item	Field_Name	Description	R/W	Step	Min	Max	Bits	Driver	Notes	CLT CNU	Status
1	PHY_Address	Which PHY is targeted	RO?	1			48	Bs	MAC address - if we use MAC address on the PHY link we will need a table of ONU MAC addresses n x 48b long. Concept implied in Motion #11 Victoria (see boyd_3bn_02_0513 slide 8).	B	R
2	Phy_Cmd_Opcode	Enumerated list of commands: NOP, Read, Write, Write/Read	RW	1	0	7	3	Bs	email thread PHY frame (in PHY-Link ad hoc folder). Implied in principle motion #11 Victoria (see boyd_3bn_02_0513 slide 8) Some questions about need for this field, may need additional details on how upper layers talk to PHY-Link.	B	R
3	Register_Address	MDIO Address of targeted register	RW	1			16	Bs	email thread PHY frame (in PHY-Link ad hoc folder). Implied in principle motion #11 Victoria (see boyd_3bn_02_0513 slide 8) Some questions about need for this field, may need additional details on how upper layers talk to PHY-Link.	B	R
4	FEC_Pointer	A pointer, in bits, to the first conplete FEC codeword in the following PHY_Link frame	RO	1	0	16383	14	T	Proposed during PHY-Link call 5/1 in EPOC-Downstream-Framing-v0.9.pdf, pointer concept implied in motion #11 Victoria. May not wish to include as to upper layers this will appear to be random.	B	R
5	FEC_Enable	A bit mapped 8 bit register to enable individual FEC code rates. Setting a bit to a logical high enable the FEC code rate. Code rate (listed from bit 0 to 8) are; RA = 8/9, RB = 8/9, RC = 0.848, RD = 3/4, RE = 9/10, RF = 9/10, RG = 13/15, and RH = 3/4.	RW	1	0	255	8	Bs	Concept proposed/implied in motion #5 from Victoria (see prodan_3bn_0513.pdf slide 6)	B	R
6	FEC_Capability	A bit mapped 8 bit register to indicate if the PHY supports the individual FEC code rates. Setting a bit to a logical high enable the FEC code rate. Code rate (listed from bit 0 to 7) are; RA = 8/9, RB = 8/9, RC = 0.848, RD = 3/4, RE = 9/10, RF = 9/10, RG = 13/15, and RH = 3/4.	RW	1	0	255	8	P	FEC concept proposed/implied in motion #5 from Victoria (see prodan_3bn_01_0513.pdf slide 6). Capability register suggesed on PHY-Link ad hoc call on5 Jun 13	B	
7	PHY_Config_ID	PHY Profile configuration in use, read only	RO	1	0	3	2	Bs	Discussed in PHY-Link ad hoc Straw Poll 10 & 11. In the CLT this may need to be a table with an entry for each CNU. Implied in Motion #11 Victoria (see boyd_3bn_02 slide 8).	B	R
8	DS OFDM Duration	Enumerated list; 20 or 40 us.	RW	1	0	1	1	B	based on carrier spacing of 25/50 us (Motion #10, Geneva)	B	
9	DS_Cyclic_Prefi	Length of DS cyclic prefix for all channels. Enumerated list {0 = .	RW	1	0	4	3	T	Aligned with and implied by Motion #26 Victoria (see pietsch_3bn_02_0313 slide 2). Changing CP is a system reregistration event.	B	

Item	Field_Name	Description	R/W	Step	Min	Max	Bits	Driver	Notes	CLT CNU	Status
10	US_Cyclic_Prefi	Length of US cyclic prefix. Enumerated list {0= 0.9375 us, 1= 1.2	RW	1	0	15	4	T	Aligned with and implied by Motion #26 Victoria (see pietsch_3bn_02_0313 slide 2). Changing CP is a system reregistration event.	B	
11	US_Resource_Block_spectrum	An enumerated list defining the number of sub-carriers in an US Resource Block. {0 = 1 SC, 1 = 2 SC, 2 = 4 SC, and 3 = 8 SC}	RW	1	0	3	2	T	Implied in motion #24 Victoria (see pietsch_3bn_01_0513 slide 3, 4), may been additional details/refinment.	B	
12	US_Resource_Block_duration	The number of symbols in an US Resource Block from 1 to 17. When FFT size = 8k the maximum value is 17, when FFT size = 4k them maximum value is 9	RW	1	1	17	5	T	Implied in motion #24 Victoria (see pietsch_3bn_01_0513 slide 3, 4), may been additional details/refinment.	B	
13	US_Resource_Block_Pilot_Spacing	The Pilot spacing in an US Resource Block from tbd to tbd	RW	tbd	tbd	tbd	#VALUE!	T	Implied in motion #24 Victoria (see pietsch_3bn_01_0513 slide 3, 4), may been additional details/refinment.	B	
14	DS_PLC_Center_Frequency_#1	Location of the DS PHY-Link center frequency from lower edge of RF Channel. In MHz from 1 to 192 in steps of 1 Mhz.	RW	1	1	192	8	Bs	Discussed in PHY-Link ad hoc 3/27. Implied in Motion #13 Victoria (see boyd_3bn_02_0513 slide 3,	B	R
15	DS_PLC_Cycle_Time_#1	The PHY_Link cycle time, in symbols from tbd to tbd symbols.	RW	1	tbd	tbd	#VALUE!	Bs	Discussed in PHY-Link ad hoc 3/27. Implied in Motion #13 Victoria (see boyd_3bn_02_0513 slide 6)	B	R
16	DS_PLC_Internal_Guard_time_#1	Amount of guard time, in symbols, internal to the PHY-Link cycle.	RW	1	0	tbd	#VALUE!	Bs	Discussed in PHY-Link ad hoc 3/27. Implied in Motion #13 Victoria (see boyd_3bn_02_0513 slide 5)	B	R
17	DS_PLC_Ending_Guard_time_#1	Amount of guard time, in symbols, at the end of of the PHY-Link cycle	RW	1	1	tbd	#VALUE!	Bs	Discussed in PHY-Link ad hoc 3/27. Implied in Motion #13 Victoria (see boyd_3bn_02_0513 slide 5)	B	R
18	DS_PLC_CRC_Errors_#1	Number of CRC Errors since MMD reset or last read (i.e, clear on read).	RW	1	0	tbd	#VALUE!	P	Based on Motion #13 Victoria (see boyd_3bn_02_0513 slide 8), Rationalized with previous CRC Error counter techniques.	B	R
19	DS_PLC_FEC_Corrected_Errors_#1	Number of FEC Correctable Errors since MMD reset or last read (i.e, clear on read).	RW	1	0	tbd	#VALUE!	P	Based on Motion #13 Victoria (see boyd_3bn_02_0513 slide 8). Rationalized with previous CRC Error counter techniques.	B	R
20	DS_PLC_FEC_Uncorrected_Errors_#1	Number of FEC uncorrectable Errors since MMD reset or last read (i.e, clear on read).	RW	1	0	tbd	#VALUE!	P	Based on Motion #13 Victoria (see boyd_3bn_02_0513 slide 8). Rationalize with previous CRC Error counter techniques.	B	R
21	DS_PLC_Srch_Freq_Start	Frequency at which to start looking for the PLC Channel . From 1 to 5000 MHz in 1 MHz steps	RW	1	1	5000	13	Bs	Discussed in PHY-Link ad hoc 5/1 and presented in Victoria, Implied in Motion #13 Victoria (see boyd_3bn_02_0513 slide 3 & 4).	U	R
22	DS_PLC_Srch_Freq_Step	Step frequency to use for PLC search. From 1 to 256 MHz in 1 MHz steps	RW	1	1	256	8	Bs	Discussed in PHY-Link ad hoc 5/1 and presented in Victoria, Implied in Motion #13 Victoria (see boyd_3bn_02_0513 slide 3 & 4).	U	R
23	DS_PLC_Srch_Cnt	Number of grid steps in search range	RW	1	1	5000	13	Bs	Discussed in PHY-Link ad hoc 5/1 and presented in Victoria, Implied in Motion #13 Victoria (see boyd_3bn_02_0513 slide 3 & 4).	U	R

Item	Field_Name	Description	R/W	Step	Min	Max	Bits	Driver	Notes	CLT CNU	Status
24	DS_PLC_Srch_Cntrl	Start and Stop a search	RW	1	0	1	1	Bs	Discussed in PHY-Link ad hoc 5/1 and presented in Victoria, Implied in Motion #13 Victoria (see boyd_3bn_02_0513 slide 3 & 4).	U	R
25	DS_PLC_Srch_Status	Indicates a completed search and successful or unsuccessful	RO	1	0	3	2	Bs	Discussed in PHY-Link ad hoc 5/1 and presented in Victoria, Implied in Motion #13 Victoria (see boyd_3bn_02_0513 slide 3 & 4).	U	R
26	DS_Center_Freq_Ch1	96 to 4904 MHz in 1 MHz steps. This eqates to channel bounds of 0 to 5000 Mhz. Permissable lower bound TDB.	RW	1	96	4904	13	T	1 MHz steps & upper bound of 5G agreed in Motion #17 Orlando	B	
27	DS_Internal_Exclusion_band_1_Start_Ch1	Internal Exclusion band lower limit, in sub-carriers; 0 to 8192 sub-carriers in steps of 1	RW	1	1	8192	13	P	Aligned with and Implied by motion #15, 17, 19, & 20 Victoria. Still need to determine minimum step size.	B	
28	Sbu-Carrier_PreEqualization	Pre-equalization in dB from tbd to tbd from nomiinal in tbd dB steps	RO	tbd	tbd	tbd	#VALUE!	P	See Motion # 27 Victoria. Pre-equalization agreed but no details provided.	U	

New/Modified text
Existing Text

Status		CLT CNU	
Idea	I	CLT CNU	T
Proposed	P	CLT CNU	U
Straw Polled	St	Both	B
Technical Decission	T	**Status**	
Baseline Starting point	Bs	Reviewed	R
Baselined	B	Straw Polled	S
Rejected	R	Motioned	M