Item	Field Name	Description	R/W	Step	Min	Max	Bits	Status	Notes	CLT CNU
1	PHY_Address	Which PHY is targeted	RO?	1			48	M	MAC address - if we use MAC address on the PHY link we will need a table of ONU MAC addresses n x 48b long. Concept implied in Motion #11 Victoria (see boyud_3bn_02_0513 slide 8).	B
2	Phy_Cmd_Opcode	Enumerated list of commands: NOP, Read, Write, Write/Read	RW	1	0	7	3	M	email thread PHY frame (in PHY-Link ad hoc folder). Implied in principle motion #11 Victoria (see boyd_3bn_02_0513 slide 8)	B
3	Register_Address	MDIO Address of targeted register	RW	1			16	M	email thread PHY frame (in PHY-Link ad hoc folder). Implied in principle motion #11 Victoria (see boyd_3bn_02_0513 slide 8)	B
4	FEC_Pointer	A pointer, in bits, to the first conplete FEC codeword in the following PHY_Link frame	RO	1	0	16383	14	M	Proposed during PHY-Link call 5/1 in EPOC-Downstream-Framing-v0.9.pdf, pointer concept implied in motion #11 Victoria.	B
5	FEC_Enable	A bit mapped 8 bit register to enable individual FEC code rates. Setting a bit to a logical high enable the FEC code rate. Code rate (listed from bit 0 to 8) are; RA = 8/9, RB = 8/9, RC = 0.848, RD = 3/4, RE = 9/10, RF = 9/10, RG = 13/15, and RH = 3/4.	RW	1	0	255	8	M	Concept proposed/implied in motion #5 from Victoria (see prodan_3bn_0513.pdf slide 6)	B
6	PHY_Config_ID	PHY Profile configuration in use, read only	RO	1	0	3	2	M	Discussed in PHY-Link ad hoc Straw Poll 10 & 11. In the CLT this may need to be a table with an entry for each CNU. Implied in Motion #11 Victoria (see boyd_3bn_02 slide 8).	B
7	DS_Cyclic_Prefix_leng	Length of DS cyclic prefix for all channels. Enumerated list {0 =	RW	1	0	4	3	B	Aligned with and implied by Motion #26 Victoria (see pietsch_3bn_02_0313 slide 2). Changing CP is a system reregistration event.	B
8	US_Cyclic_Prefix_leng	Length of US cyclic prefix. Enumerated list {0= 0.9375 us, 1= 1.2	RW	1	0	15	4	B	Aligned with and implied by Motion #26 Victoria (see pietsch_3bn_02_0313 slide 2). Changing CP is a system reregistration event.	B
9	US_Resource_Block_spectrum	An enumerated list defining the number of sub-carriers in an US Resource Block. {0 = 1 SC, 1 = 2 SC, 2 = 4 SC, and 3 = 8 SC}	RW	1	0	3	2	P	Implied in motion #24 Victoria (see pietsch_3bn_01_0513 slide 3, 4), may been additional details/refinment.	B
10	US_Resource_Block_duration	The number of symbols in an US Resource Block from 1 to 17. When FFT size = 8k the maximum value is 17, when FFT size = 4k them maximum value is 9	RW	1	1	17	5	P	Implied in motion #24 Victoria (see pietsch_3bn_01_0513 slide 3, 4), may been additional details/refinment.	B
11	US_Resource_Block_Pilot_Spacing	The Pilot spacing in an US Resource Block from tbd to tbd	RW	tbd	tbd	tbd	#VALUE!	P	Implied in motion #24 Victoria (see pietsch_3bn_01_0513 slide 3, 4), may been additional details/refinment.	B
12	PLC_Center_Frequency	Location of the DS PHY-Link center frequency from lower edge of RF Channel. In MHz from 1 to 192 in steps of 1 Mhz.	RW	1	1	192	8	B	Discussed in PHY-Link ad hoc 3/27. Implied in Motion #13 Victoria (see boyd_3bn_02_0513 slide 3,	B

Item	Field Name	Description	R/W	Step	Min	Max	Bits	Status	Notes	CLT CNU
13	PLC_Cycle_Time	The PHY_Link cycle time, in symbols from tbd to tbd symbols.	RW	1	tbd	tbd	#VALUE!	B	Discussed in PHY-Link ad hoc 3/27. Implied in Motion #13 Victoria (see boyd_3bn_02_0513 slide 6)	B
14	PLC_Internal_Guard_time	Amount of guard time, in symbols, internal to the PHY-Link cycle.	RW	1	0	tbd	#VALUE!	B	Discussed in PHY-Link ad hoc 3/27. Implied in Motion #13 Victoria (see boyd_3bn_02_0513 slide 5)	B
15	PLC_Ending_Guard_time	Amount of guard time, in symbols, at the endof of the PHY-Link cycle	RW	1	1	tbd	#VALUE!	B	Discussed in PHY-Link ad hoc 3/27. Implied in Motion #13 Victoria (see boyd_3bn_02_0513 slide 5)	B
16	PLC_CRC_Errors	Number of CRC Errors in the most recent period (tbd time)	RW	1	0	tbd	#VALUE!	P	Based on Motion #13 Victoria (see boyd_3bn_02_0513 slide 8)	B
17	PLC_FEC_Corrected_Errors	Number of FEC Correctable Errors in the most recent period (tbd time)	RW	1	0	tbd	#VALUE!	P	Based on Motion #13 Victoria (see boyd_3bn_02_0513 slide 8)	B
18	PLC_FEC_Uncorrected_Errors	Number of FEC uncorrectable Errors in the most recent period (tbd time)	RW	1	0	tbd	#VALUE!	P	Based on Motion #13 Victoria (see boyd_3bn_02_0513 slide 8)	B
19	DS_PLC_Srch_Freq_Start	Frequency at which to start looking for the PLC Channel . From 1 to 5000 MHz in 1 MHz steps	RW	1	1	5000	13	B	Discussed in PHY-Link ad hoc 5/1 and presented in Victoria, Implied in Motion #13 Victoria (see boyd_3bn_02_0513 slide 3 & 4).	U
20	DS_PLC_Srch_Freq_Step	Step frequency to use for PLC search. From 1 to 256 MHz in 1 MHz steps	RW	1	1	256	8	B	Discussed in PHY-Link ad hoc 5/1 and presented in Victoria, Implied in Motion #13 Victoria (see boyd_3bn_02_0513 slide 3 & 4).	U
21	DS_PLC_Srch_Cnt	Number of grid steps in search range	RW	1	1	5000	13	B	Discussed in PHY-Link ad hoc 5/1 and presented in Victoria, Implied in Motion #13 Victoria (see boyd_3bn_02_0513 slide 3 & 4).	U
22	DS_PLC_Srch_Cntrl	Start and Stop a search	RW	1	0	1	1	B	Discussed in PHY-Link ad hoc 5/1 and presented in Victoria, Implied in Motion #13 Victoria (see boyd_3bn_02_0513 slide 3 & 4).	U
23	DS_PLC_Srch_Status	Indicates a completed search and successful or unsuccessful	RO	1	0	3	2	B	Discussed in PHY-Link ad hoc 5/1 and presented in Victoria, Implied in Motion #13 Victoria (see boyd_3bn_02_0513 slide 3 & 4).	U
24	DS_Ch_Center_Freq	96 to 4904 MHz in 1 MHz steps. This eqates to channel bounds of 96 to 4904 Mhz. Permissable lower bound TDB.	RW	1	96	4904	13	B	1 MHz steps & upper bound of 5G agreed in Motion #17 Orlando	B
25	DS_CH_Internal_Exclusion_band_1_Start	Internal Exclusion band lower limit, in sub-carriers; 0 to 8192 sub-carriers in steps of 1	RW	1	1	8192	13	P	Aligned with and Implied by motion #15, 17, 19, & 20 Victoria. Still need to determine minimum step size.	B
26	Sub-Carrier_PreEqualization	Pre-equalization in dB(?) from tbd to tbd from nomiinal in tbd dB steps	RO	tbd	tbd	tbd	#VALUE!	P	See Motion # 27 Victoria. Pre-equalization agreed but no details provided.	U

CLT CNU	T
CLT CNU	U
Both	B