101.3.2.1 Idle control character deletion process

In the transmitting PCS, the Idle control character deletion process is responsible for deleting excess Idle control characters inserted in between individual frames to adjust the data rate enforced by the MAC Control (as defined in {Clause 102}) to the effective data rate supported by the PCS and PMD. The gaps created within the data stream by the operation of the Idle control character deletion process are used in one of the following ways:

a) some gaps created by the removal of Idle control characters are filled with FEC parity data (FEC overhead compensation sub-process); and

b) other gaps created by the removal of Idle control characters are discarded in order to decrease the data rate between the MAC and PHY, while maintaining the effective data rate unchanged (data rate adaptation sub-process).

The Idle control character deletion process deletes a specific number of 72-bit vectors containing Idle control characters from the data stream composed of a series of 72-bit vectors received from the XGMII. The number of deleted 72-bit vectors containing Idle control characters depends on the EPoC PMD data rate, PMD overhead (including, for example, Cyclic Prefix), and the size of FEC parity data. The Idle control character deletion process is composed of two sub-processes, executed simultaneously:

a) data rate adaptation sub-process, where the PCS discards a specific number of excess Idle control characters to decrease the data rate to match the effective data rate supported by the EPoC PMD; and

b) FEC overhead compensation sub-process, where the PCS discards the remaining excess Idle control characters to prepare space in the de-rated data stream for PHY parity data.

The operation of the EPoC MPCP defined in {Clause 102} ensures that a sufficient number of excess Idle control characters are present in the data stream, so that the minimum IPG between two adjacent frames is preserved once all excess Idle control characters are removed through the operation of the data rate adaptation and the FEC overhead compensation sub-processes.

101.3.2.1.1 Constants

FEC_DSize

TYPE: 16-bit unsigned integer
The number of 72-bit vectors constituting the payload portion of a FEC codeword. To normalize pre-FEC data rate, the Idle control character deletion process removes FEC_OSize vectors per every FEC_DSize vectors transferred to the 64b/66b encoder.
Value: {TBD}

FEC_OSize

TYPE: 16-bit unsigned integer
The number of 72-bit vectors constituting the parity (overhead) portion of a FEC codeword. To normalize pre-FEC data rate, the Idle control character deletion process removes FEC_OSize vectors per every FEC_DSize vectors transferred to the 64b/66b encoder.
Value: {TBD}

Note that the list of constants will be updated per technical decision #45 (http://www.ieee802.org/3/bn/public/decisions/decisions.html) once EPoC-specific FEC and PMD overhead details are settled.

101.3.2.1.2 Variables

BEGIN

TYPE: Boolean
This variable is used when initiating operation of the state diagram. It is set to true following initialization and every reset.

delayBound

TYPE: 16-bit unsigned integer

This value represents the delay sufficient to initiate the transmitter at the CNU and to stabilize the receiver at the CLT (i.e., the maximum FIFO size expressed in units of 66-bit blocks). The value of delayBound includes {to be added when the burst structure is known}. This variable is used only by the CNU.

PHY_DSize

TYPE: 16-bit unsigned integer

The number of 72-bit vectors constituting (together with PHY_OSize) the denominator in the EPoC PCS de-rating Equation (101–1). To normalize the effective PCS data rate, the Idle control character deletion process removes PHY_OSize vectors per every PHY_DSize vectors transferred to the 64b/66b encoder.

Value: {TBD, reference how it is calculated ?}

$$\text{PCS\_Rate} = \text{XGMII\_Rate} \times \frac{\text{PHY\_OSize}}{\text{PHY\_DSize} + \text{PHY\_OSize}} \qquad (101–1)$$

PHY_OSize

TYPE: 16-bit unsigned integer

The number of 72-bit vectors constituting the numerator in the EPoC PCS de-rating Equation (101–1). To normalize the effective PCS data rate, the Idle control character deletion process removes PHY_OSize vectors per every PHY_DSize vectors transferred to the 64b/66b encoder.

Value: {TBD, reference how it is calculated ?}

tx_raw<71:0>

This variable is defined in {49.2.13.2.2}.

tx_raw_out<71:0>

72-bit vector sent from the output of the Idle control character deletion process to the 64b/66b encoder. This vector contains two XGMII transfers mapped as shown for tx_raw<71:0>.

Note that the list of variables will be updated per technical decision #45 (http://www.ieee802.org/3/bn/public/decisions/decisions.html) once EPoC-specific FEC and PMD overhead details are settled.

101.3.2.1.3 Counters

countDelete

TYPE: 16-bit unsigned integer

Counts the number of 72-bit vectors that need to be deleted from the received data stream as part of the FEC overhead compensation and data rate adaptation sub-processes.

countIdle

TYPE: 16-bit unsigned integer

Counts the number of 72-bit vectors containing Idle control characters or other control vectors as part of the FEC overhead compensation and data rate adaptation sub-processes.

countVector

TYPE: 16-bit unsigned integer

Counts the number of 72-bit vectors transmitted after the removal of Idle characters as part of the FEC overhead compensation and data rate adaptation sub-processes.

Note that the list of counters will be updated per technical decision #45 (http://www.ieee802.org/3/bn/pub-

lic/decisions/decisions.html) once EPoC-specific FEC and PMD overhead details are settled.

101.3.2.1.4 Functions

T_TYPE(tx_raw<71:0>)
This function is defined in {49.2.13.2.3}.

Note that the list of functions will be updated per technical decision #45 (http://www.ieee802.org/3/bn/public/decisions/decisions.html) once EPoC-specific FEC and PMD overhead details are settled.

101.3.2.1.5 State diagrams

The CLT PCS shall perform the Idle control character deletion process as shown in Figure 101–1, covering both the data rate adaptation and FEC overhead compensation sub-processes. The CNU PCS shall perform the Idle control character deletion process as shown in Figure 101–2, covering both the data rate adaptation and FEC overhead compensation sub-processes.

In case of any discrepancy between state diagrams and the descriptive text, the state diagrams prevail.

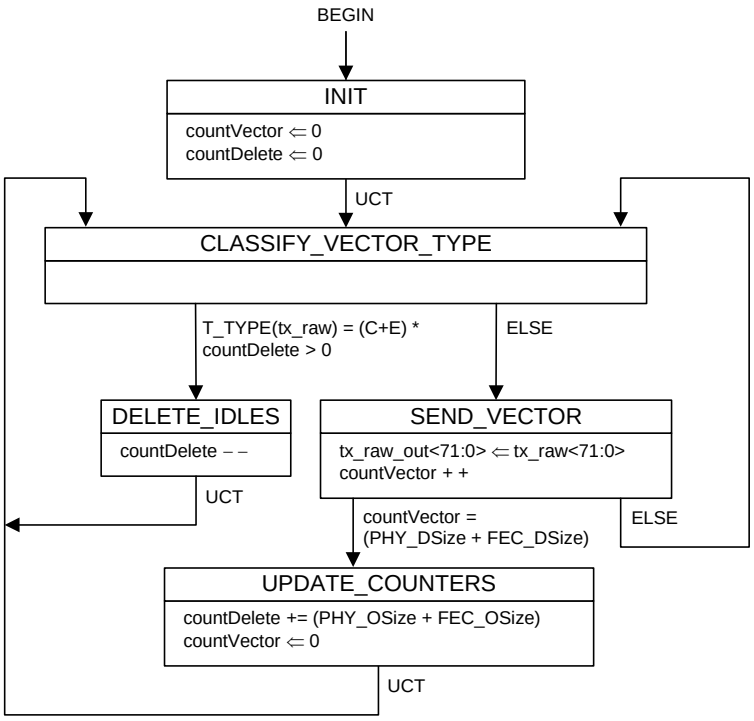

Figure 101–1—CLT Idle control character deletion process

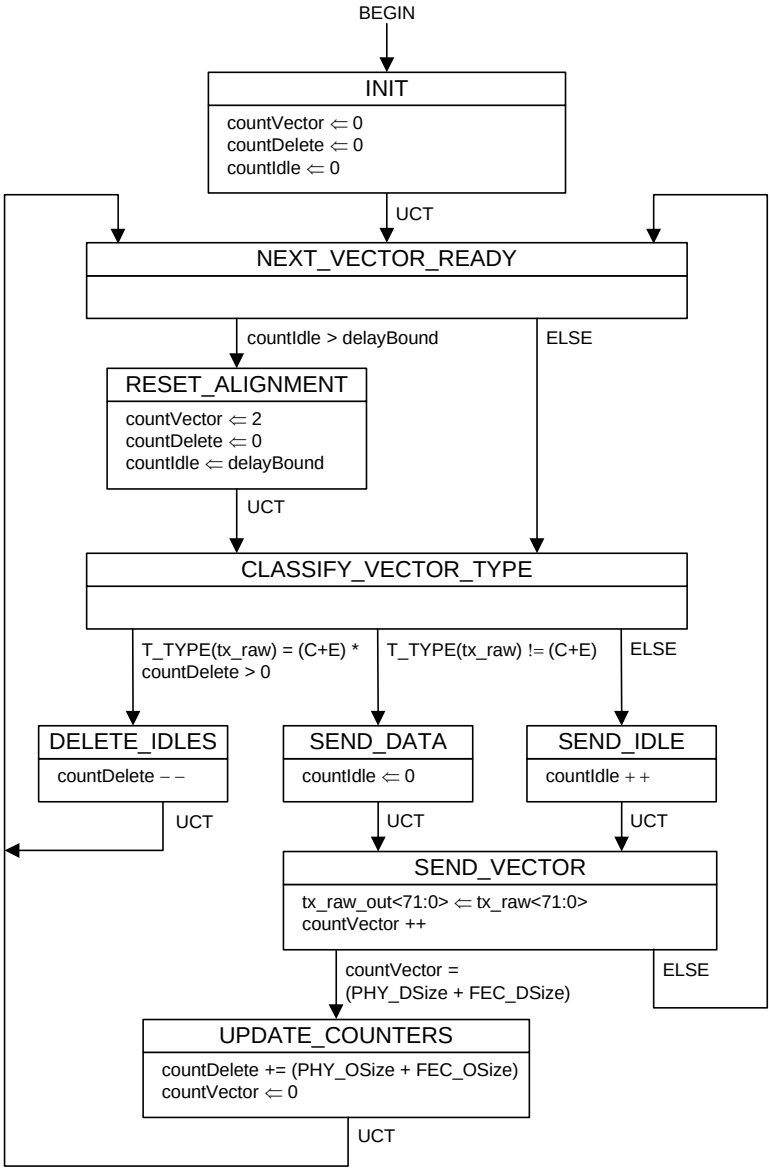

Figure 101–2—CNU Idle control character deletion process

Note that Figure 101–1 and Figure 101–2 will be updated per technical decision #45 (http://www.ieee802.org/3/bn/public/decisions/decisions.html) once EPoC-specific FEC and PMD overhead details are settled, as well as the burst structure is defined.

101.3.3.7 Idle control character insertion process

In the receiving PCS, the Idle control character insertion process inserts Idle control characters into the data stream with gaps as received from the FEC decoder and 64b/66b decoder, adjusting the effective PCS and PMD data rate to the data rate enforced by the MAC Control (as defined in {Clause 102}). Effectively, the Idle control character insertion process fills in the gaps created after the removal of FEC parity data, as well as compensates for the derating of the EPoC PMD relative to the EPoC MAC.

The Idle control character insertion process (see {Figure 101-3}) is composed of:

a) a receive process, receiving 72-bit vectors from the 64b/66b decoder and writing them into the Idle Insertion FIFO (called FIFO_II); and

b) a transmit process, reading 72-bit vectors from FIFO_II and transferring them to the XGMII.

The receive process receives 72-bit vectors from the 64b/66b decoder at a slower data rate than the nominal XGMII data rate for two reasons:

a) the FEC parity data is removed within the FEC decoder, leaving behind gaps in the data stream; and

b) the data rate supported by EPoC PCS and PMD is lower than the data rate supported by MAC Control Client, requiring data rate adaptation between the PCS and MAC.

The transmit process outputs 72-bit vectors at the nominal XGMII data rate.

To match the difference in data rates between the receive process and the transmit process, the Idle control character insertion process inserts additional 72-bit vectors containing Idle control characters. The additional blocks are inserted between frames and not necessarily at the same locations where FEC parity data was removed within the FEC decoder.

101.3.3.7.1 Constants

FIFO_II_SIZE

TYPE: 16-bit unsigned integer

This constant represents the size of Idle Insertion FIFO buffer. The size of this buffer is selected in such a way that it is able to accommodate the number of 66-bit vectors sufficient to fill the gap introduced by removing the FEC parity data for a maximum size MAC frame, and compensate for the maximum supported difference between the MAC rate and PMD rate.

Value: {TBD}

It seems that the FIFO_II_SIZE depends on the two following items: (a) the type of FEC and the size of FEC parity that is removed from data stream at regular intervals; and (b) the data rate differential between the PMD and the MAC. Every time the data rate changes, the size of FIFO_II may need to be adapted as well, to make sure that no additional delay / jitter is introduced. Whether such a change is needed, needs to be studied in more detail when more PMD/PCS details are available.

IDLE_VECTOR

TYPE: 72-bit binary array

This constant represents a 72-bit vector containing Idle control characters.

LBLOCK_R

This constant is defined in {49.2.13.2.1}.

Note that the value of FIFO_II_SIZE, as well as the list of constants will be updated per technical decision #43 and #45 (http://www.ieee802.org/3/bn/public/decisions/decisions.html) once EPoC-specific FEC and PMD overhead details are settled.

101.3.3.7.2 Variables

BEGIN

TYPE: Boolean

This variable is used when initiating operation of the state diagram. It is set to true following initialization and every reset.

FIFO_II

TYPE: Array of 72-bit vectors

The FIFO_II buffer is used to perform data rate adaptation between XGMII data rate and the EPoC PMD data rate. Upon initialization, all elements of this array are filled with instances of IDLE_VECTOR. The FIFO_II buffer has the size of FIFO_II_SIZE (see 101.3.3.7.1).

RX_CLK

TYPE: Boolean

This variable represents the RX_CLK signal defined in {46.3.2.1}.

rx_raw_in<71:0>

TYPE: 72-bit binary array

This variable represents a 72-bit vector received from the output of the 64b/66b decoder. RXD<0> through RXD<31> for the second transfer are placed in rx_raw<40> through rx_raw<71>, respectively.

rx_raw_out<71:0>

TYPE: 72-bit binary array

This variable represents a 72-bit vector passed from the Idle control character insertion process to XGMII. The vector is mapped to two consecutive XGMII transfers as follows:

Bits rx_raw<3:0> are mapped to RXC<3:0> for the first transfer;
Bits rx_raw<7:4> are mapped to RXC<3:0> for the second transfer;
Bits rx_raw<39:8> are mapped to RXD<31:0> for the first transfer;
Bits rx_raw<71:40> are mapped to RXD<31:0> for the second transfer.

countVector

TYPE: 16-bit unsigned integer

This variable represents the number of 72-bit vectors stored in the FIFO_II at the given moment of time.

101.3.3.7.3 Functions

T_TYPE(rx_raw<71:0>)

This function is defined in {49.2.13.2.3}.

101.3.3.7.4 Messages

DECODER_UNITDATA.indicate(rx_raw_in<71:0>)

A signal sent by the EPoC PCS Receive process, conveying the next received 72-bit vector.

DUDI

Alias for DECODER_UNITDATA.indicate(rx_raw_in<71:0>).

101.3.3.7.5 State diagrams

The CLT and CNU PCS shall perform the Idle control character insertion process as shown in Figure 101–3. In case of any discrepancy between state diagrams and the descriptive text, the state diagrams prevail.

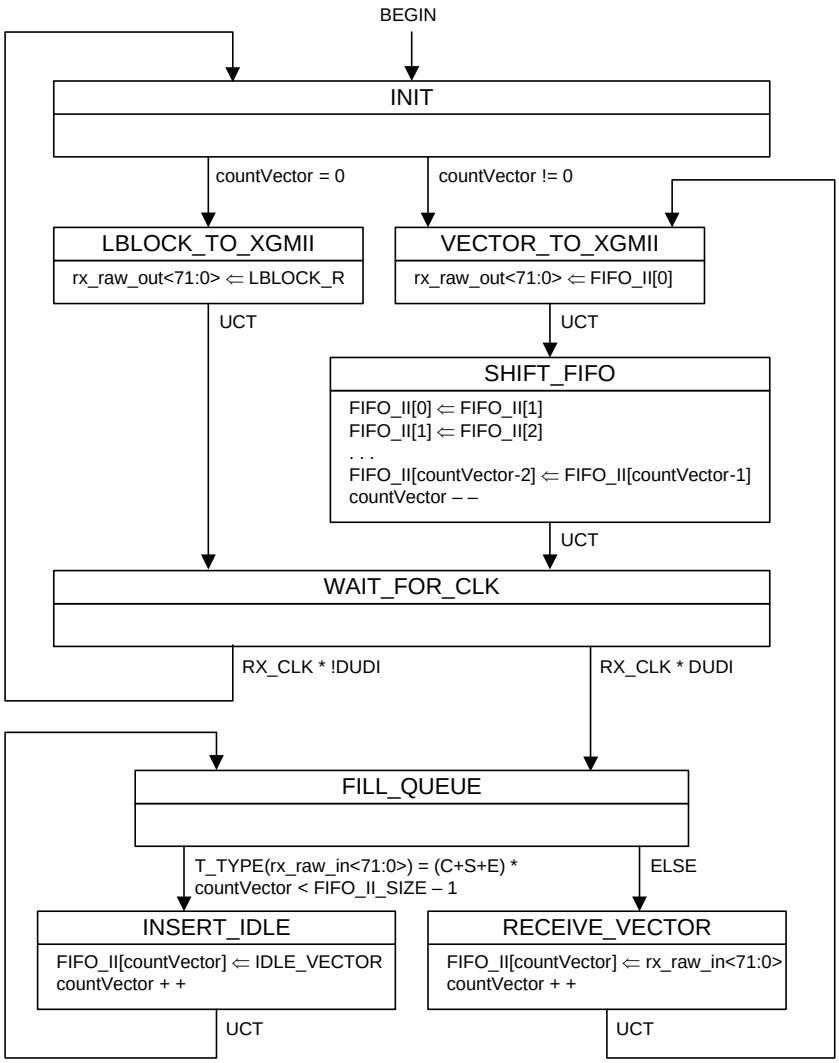

Figure 101–3—Idle control character insertion process state diagram