Technical Feasibility of 100G Designs

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April, 2007

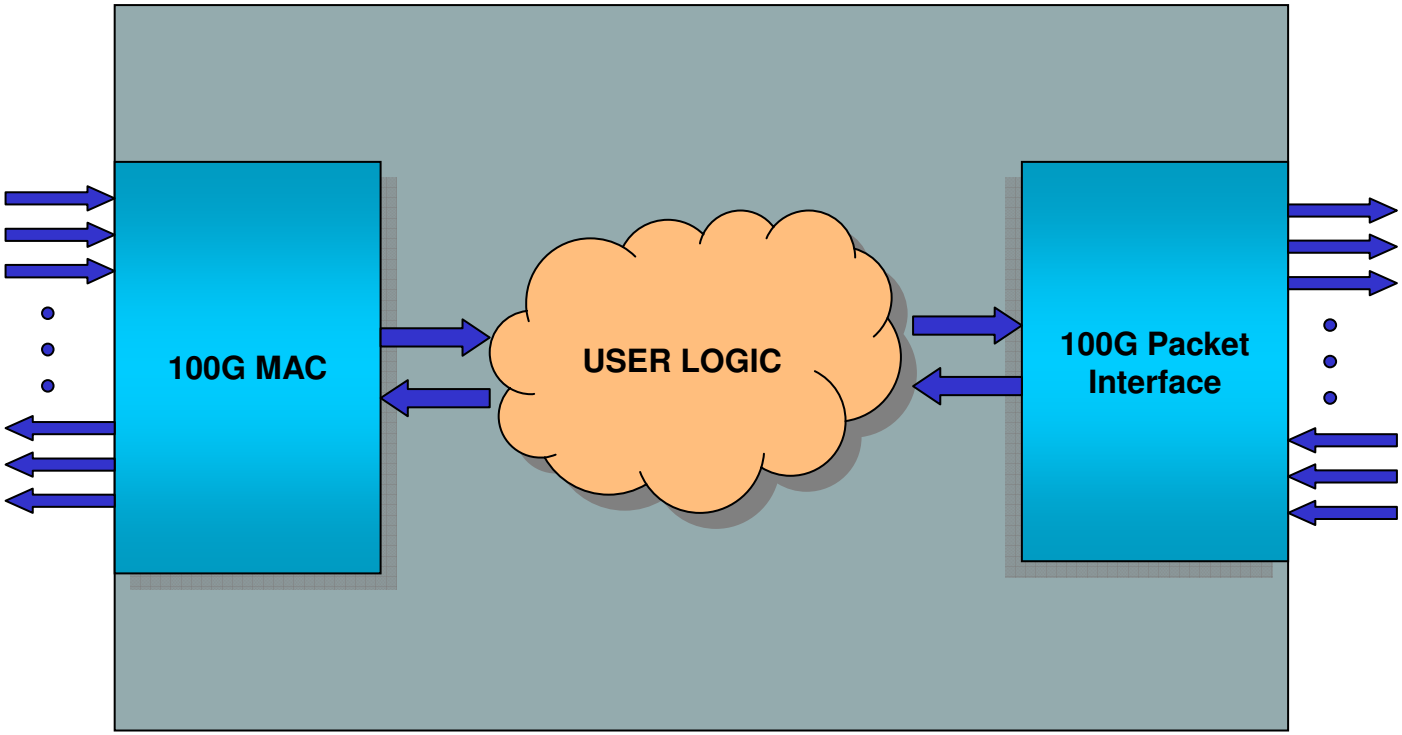
Outline

- Presentation is focused on the implementation of the digital cores

- Agenda:
  - 100G Devices
  - 120G Interlaken Interface
  - Comparison to 100G MAC proposals
  - Conclusions

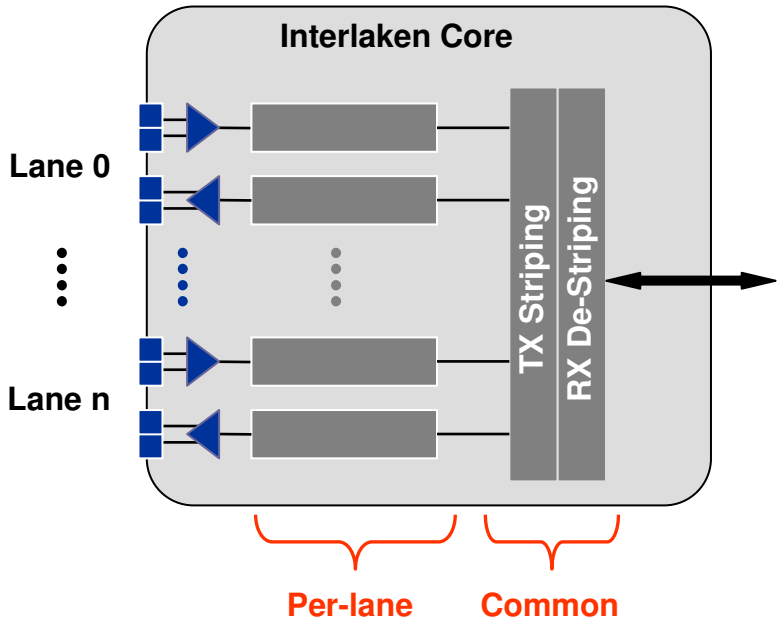
100G Devices

- Need to keep in mind that there are two interfaces per devices



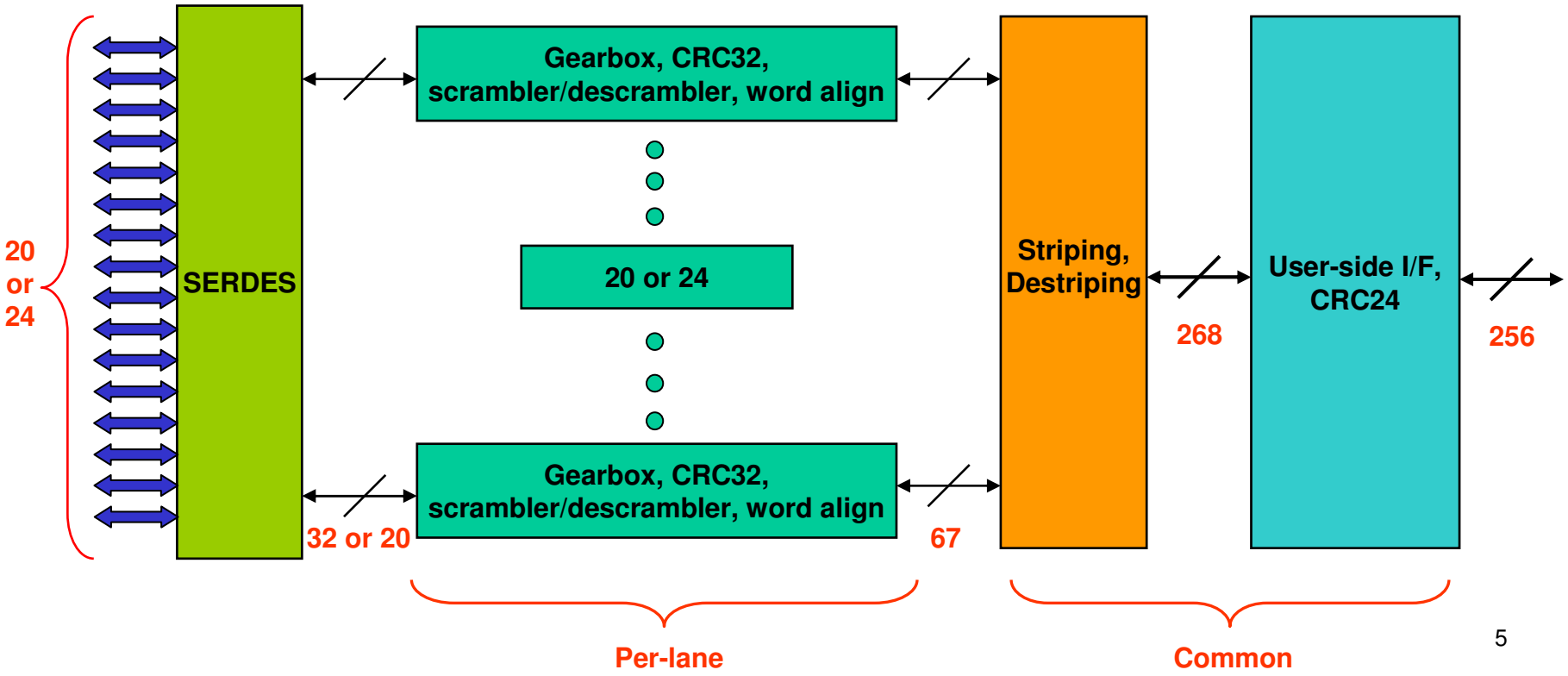
Interlaken Overview

- Interlaken: protocol for chip-2-chip packet interface
- Interlaken concepts:
  - Can use any SERDES technology
  - Scalable over any number of serial lanes
  - Operation divided into two distinct sections:
    1. Per-lane logic
    2. Common logic



120G Interlaken Implementation

- Configuration:
  - 20 lanes @ 6.25 Gbps (125G raw bandwidth)
  - 24 lanes @ 5 Gpbs (120G raw bandwidth)

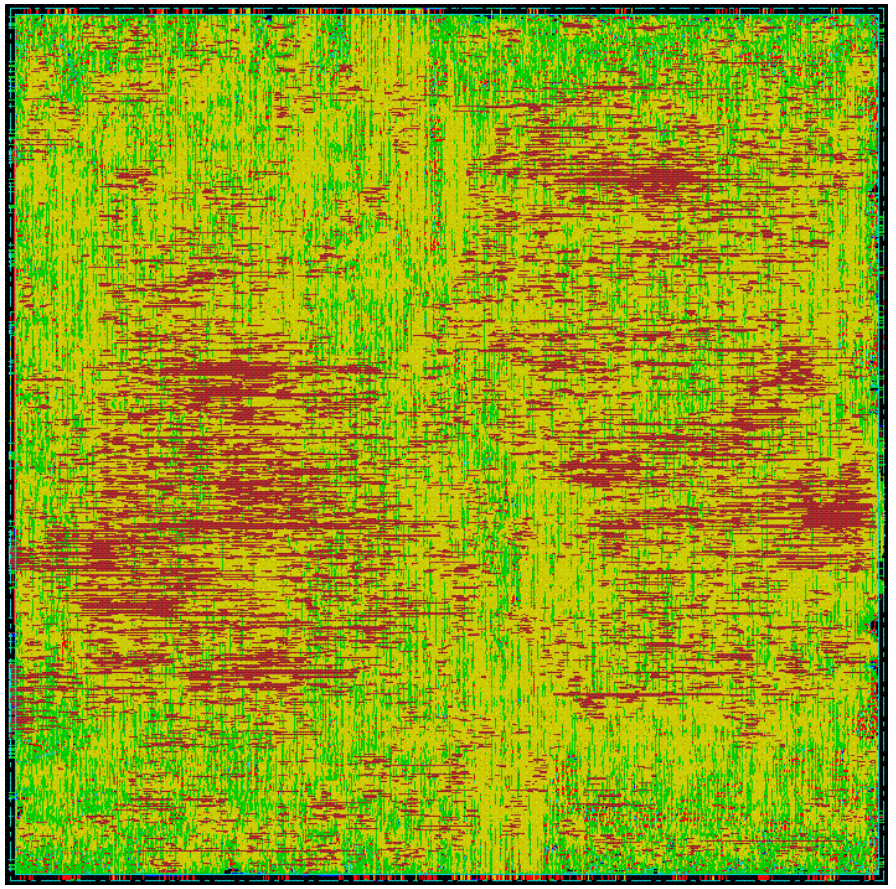


SARANCE TECHNOLOGIES

ASIC Implementation Details

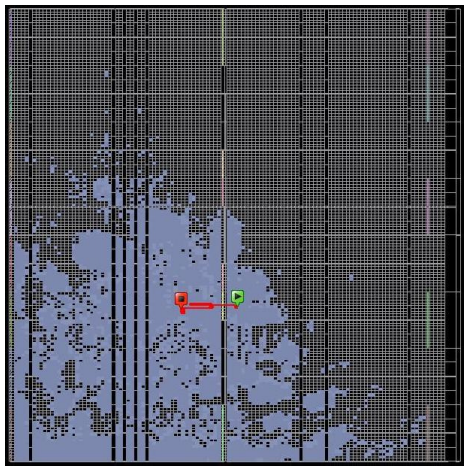
90nm CMOS technology

- **Internal bus width:**
  - **268 bits**
- **20 lanes:**
  - **470 MHz core clock**
- **24 lanes:**
  - **450 MHz core clock**
- **Gate count:**
  - **~600K gates for 24 lane core**

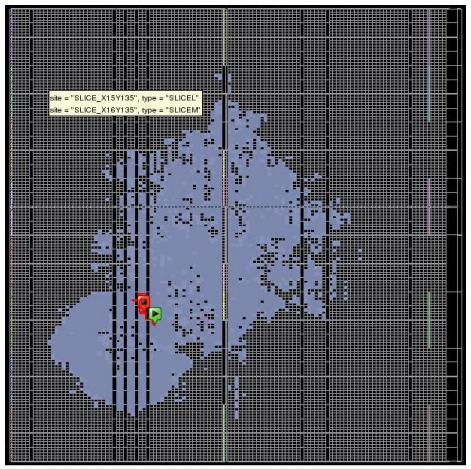


FPGA Implementation Details

Receiver



Transmitter



65nm FPGA technology

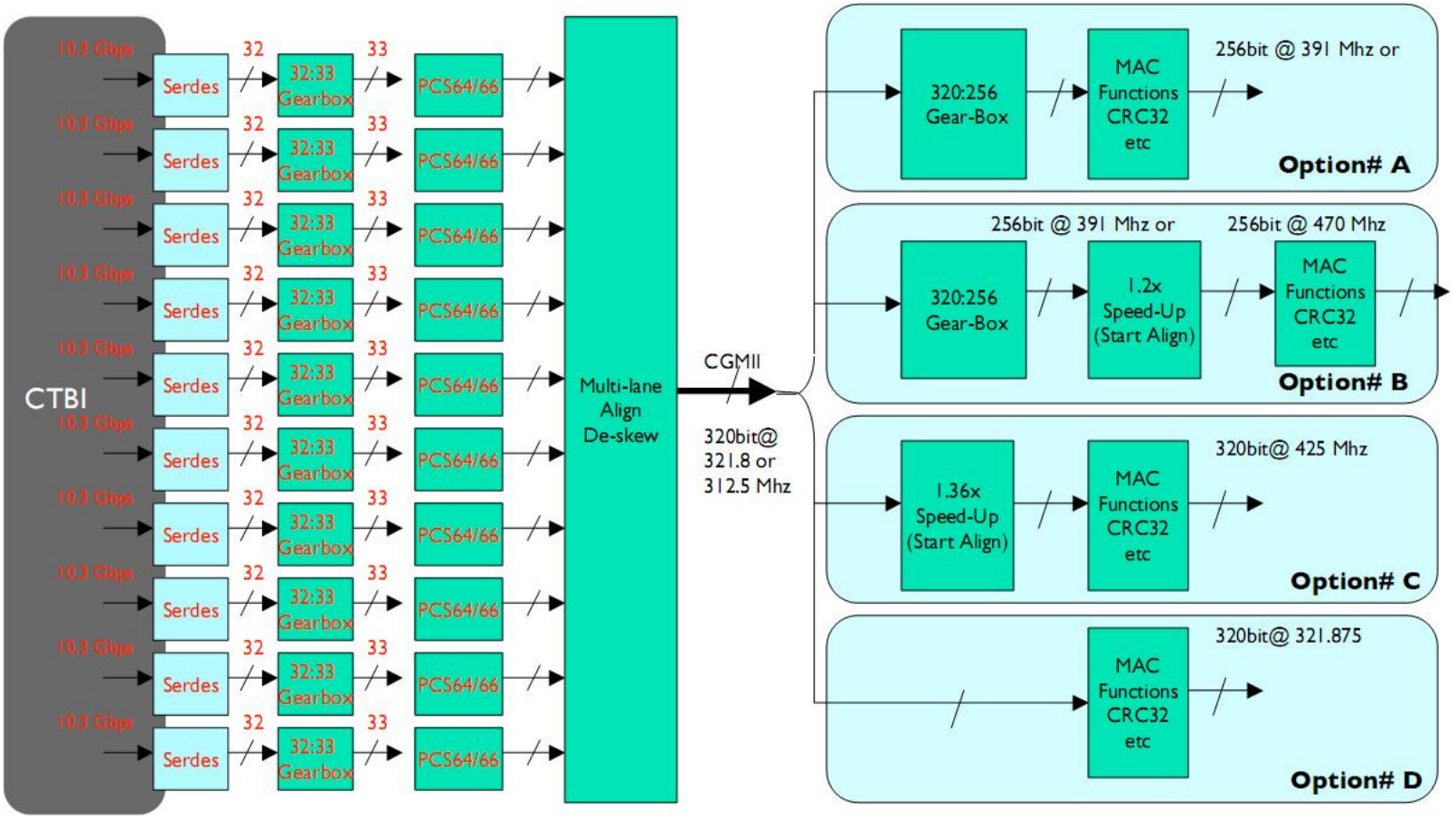
- **Internal bus width:**
  - **536 bits**
- **20 lanes:**
  - **235 MHz core clock**
- **24 lanes:**
  - **225 MHz core clock**

- **Utilization:**
  - **45K LUTs and 650 RAM32M blocks for 24 lane core**

Target Device: Xilinx Virtex™ 5 family

100G PCS/MAC Receiver

source: belhadj_01_1106-1 presentation given in November 2006



SARANCE TECHNOLOGIES

Comparing Interlaken and 100G MAC/PCS

- Common logic
  - Interlaken: CRC24, user-side interface
  - 100G MAC/PCS: CRC32, user-side interface
- Striping/De-striping
  - Interlaken: stripe over any number of lanes
  - 100G MAC/PCS: stripe over virtual lanes
- Per-lane logic
  - Interlaken: gearbox, scrambler/descrambler, 64/67 encode/decode, CRC32, word align
  - 100G MAC/PCS: gearbox, 64/66 encode/decode, word align

Similar at a high level

Comparing 120G Interlaken and 100G MAC/PCS

Criteria	120G Interlaken	100G MAC/PCS*	Comments
Common logic	- CRC24 is 64-bit aligned - User I/F @ 450MHz	- CRC32 is 8-bit aligned - User I/F @ 391MHz	CRC32 is more complex but feasible**
Striping/de-striping	256 bit bus <-> 24 lanes	256 bit bus <-> 20 virtual lanes	Similar complexity
Per lane logic	gearbox, scrambler/descrambler, 64/67 encode/decode, CRC32, word align	gearbox, 64/66 encode/decode, word align	Similar complexity

* - source: belhadj_01_1106-1 presentation given in November 2006
** - CRC32 size is 400K gates for both receiver and transmit

Logic complexity is similar

Conclusions

- 120G Interlaken already implemented in ASIC and FPGA technology
  - Two different implementations were discussed:
    - 20 lanes @ 6.25 Gbps
    - 24 lanes @ 5 Gpbs
- 120G Interlaken and 100G MAC/PCS are of similar logic complexity
- Logic complexity is manageable and should not be the main criteria for defining 100G MAC/PCS protocol
  - The number of virtual lanes does not need to be a power of 2 as long as the base word size is a multiple of 8 bits
- Focus should be on SERDES technology, risk management and power reduction