How can 40 Gb Ethernet be designed to fit existing ODU3 transport?

IEEE HSSG Meeting, San Francisco — July 16-19, 2007

Stephen J. Trowbridge
Chief Technology Office – Optics Division
Alcatel-Lucent

Supporters

- Pete Anslow (Nortel Networks)
- Thomas Fischer (Nokia Siemens Networks)
- Ted Woodward (Telcordia)
- Matt Traverso (Optnext)
- Yann Loussouarn (France Telecom Orange)
- Ralf-Peter Braun (Deutsche Telekom T-Systems)
- Ghani Abbas (Ericsson)
- Med Belhadj (Cortina Systems)
- Frank Chang (Vitesse)
- Martin Carroll (Verizon)
- Keith Conroy (AMCC)

How can an encoded line rate of 40.149716 Gbit/s or less be achieved for 40 Gb Ethernet?

An encoded line rate of 40.149716 Gbit/s or less is needed to allow bit transparent transport via standard OPU3 (see duelk_01_0707.pdf)

Alternatives to be considered:

- **Option 1**: Reduce the MAC/PLS rate to 38.9 Gbit/s (or a round number like 38 Gbit/s) and continue to use 64B/66B coding
- **Option 2**: Keep the MAC/PLS rate at 40G and develop a more economical PCS line code that requires less than 0.36425% of overhead
- **Option 3**: Use a combination of a lower MAC/PLS rate and a more economical PCS line code so that the encoded line rate is less than 40.149716 Gbit/s
- **Option 4**: Packet level encoding – don't put all of the preamble or IFG in the encoded signal to try to reduce the encoded line rate to less than 40.149716 Gbit/s

Option 1:
Lower MAC/PLS Rate of 38.9 Gb/s

OPU3 payload rate	40.150 519 322 Gbit/s ±20ppm
-20ppm	40.149 716 312 Gbit/s
MAC Rate	38.9 Gbit/s ±100ppm
+100ppm	38.903 890 Gbit/s
With 64B/66B Coding	40.119 636 563 Gbit/s

Option 2: Could a more economical linecode be developed with <=0.36425% overhead?

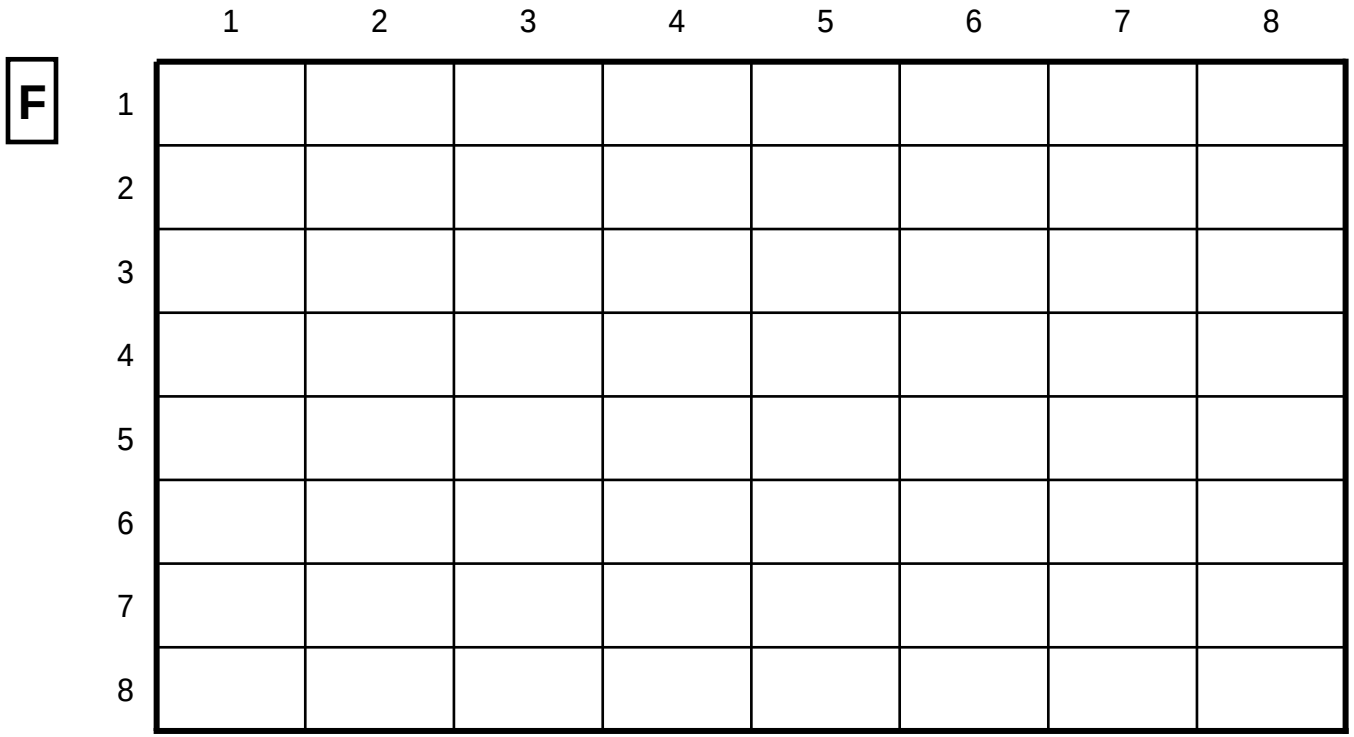
Input Data	Sync	Block Payload							
Bit Position: / Data Block Format:	0 1	2							65
$D_0\,D_1\,D_2\,D_3/D_4\,D_5\,D_6\,D_7$	01	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
Control Block Formats:		Block Type Field							
$C_0\,C_1\,C_2\,C_3/C_4\,C_5\,C_6\,C_7$	10	0x1e	C_0	C_1	C_2	C_3	C_4	C_5	C_6	C_7
$C_0\,C_1\,C_2\,C_3/O_4\,D_5\,D_6\,D_7$	10	0x2d	C_0	C_1	C_2	C_3	O_4	D_5	D_6	D_7
$C_0\,C_1\,C_2\,C_3/S_4\,D_5\,D_6\,D_7$	10	0x33	C_0	C_1	C_2	C_3		D_5	D_6	D_7
$O_0\,D_1\,D_2\,D_3/S_4\,D_5\,D_6\,D_7$	10	0x66	D_1	D_2	D_3	O_0		D_5	D_6	D_7
$O_0\,D_1\,D_2\,D_3/O_4\,D_5\,D_6\,D_7$	10	0x55	D_1	D_2	D_3	O_0	O_4	D_5	D_6	D_7
$S_0\,D_1\,D_2\,D_3/D_4\,D_5\,D_6\,D_7$	10	0x78	D_1	D_2	D_3	D_4		D_5	D_6	D_7
$O_0\,D_1\,D_2\,D_3/C_4\,C_5\,C_6\,C_7$	10	0x4b	D_1	D_2	D_3	O_0	C_4	C_5	C_6	C_7
$T_0\,C_1\,C_2\,C_3/C_4\,C_5\,C_6\,C_7$	10	0x87		C_1	C_2	C_3	C_4	C_5	C_6	C_7
$D_0\,T_1\,C_2\,C_3/C_4\,C_5\,C_6\,C_7$	10	0x99	D_0		C_2	C_3	C_4	C_5	C_6	C_7
$D_0\,D_1\,T_2\,C_3/C_4\,C_5\,C_6\,C_7$	10	0xaa	D_0	D_1		C_3	C_4	C_5	C_6	C_7
$D_0\,D_1\,D_2\,T_3/C_4\,C_5\,C_6\,C_7$	10	0xb4	D_0	D_1	D_2		C_4	C_5	C_6	C_7
$D_0\,D_1\,D_2\,D_3/T_4\,C_5\,C_6\,C_7$	10	0xcc	D_0	D_1	D_2	D_3		C_5	C_6	C_7
$D_0\,D_1\,D_2\,D_3/D_4\,T_5\,C_6\,C_7$	10	0xd2	D_0	D_1	D_2	D_3	D_4		C_6	C_7
$D_0\,D_1\,D_2\,D_3/D_4\,D_5\,T_6\,C_7$	10	0xe1	D_0	D_1	D_2	D_3	D_4	D_5		C_7
$D_0\,D_1\,D_2\,D_3/D_4\,D_5\,D_6\,T_7$	10	0xff	D_0	D_1	D_2	D_3	D_4	D_5	D_6	

Figure 49–7—64B/66B block formats

Current 64B/66B coding used in 10GBase-R (IEEE 802.3-2005, Clause 49)

Option 2: Possible 512-bit/513-bit coding
Reuse concept of 64-bit/65-bit coding of GFP-T

8 x 8 octet frame with one “Flag” bit indicating the presence of control blocks



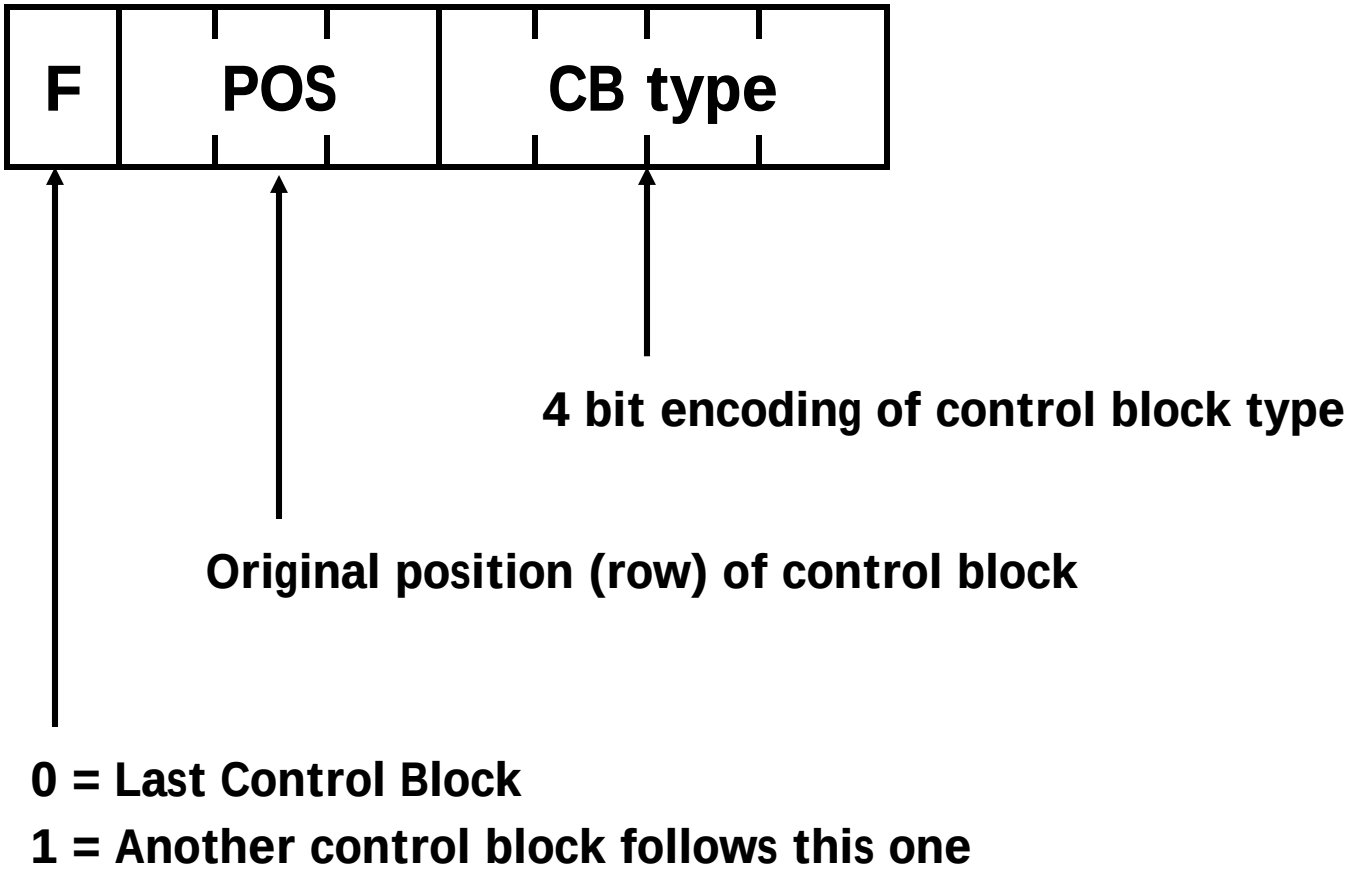
Alcatel·Lucent

Option 2:
4 bit encoding of 64B/66B control block type

Type	4 bit code
0x1e	0001
0x2d	0010
0x33	0011
0x66	0100
0x55	0101
0x78	0110
0x4b	0111
0x87	1000

Type	4 bit code
0x99	1001
0xaa	1010
0xb4	1011
0xcc	1100
0xd2	1101
0xe1	1110
0xff	1111

Option 2:
Control Block header byte



Option 2:
Example – All data blocks

0	1	2	3	4	5	6	7	8
1	D	D	D	D	D	D	D	D
2	D	D	D	D	D	D	D	D
3	D	D	D	D	D	D	D	D
4	D	D	D	D	D	D	D	D
5	D	D	D	D	D	D	D	D
6	D	D	D	D	D	D	D	D
7	D	D	D	D	D	D	D	D
8	D	D	D	D	D	D	D	D

Option 2:
Example – One control block, Seven all-data blocks

aaa = original row of control block

cccc = 4 bit encoding of control block type

X X X X X X X = per format of 64B/66B control block type

1

	1	2	3	4	5	6	7	8
1	0aaacccc	X	X	X	X	X	X	X
2	D	D	D	D	D	D	D	D
3	D	D	D	D	D	D	D	D
4	D	D	D	D	D	D	D	D
5	D	D	D	D	D	D	D	D
6	D	D	D	D	D	D	D	D
7	D	D	D	D	D	D	D	D
8	D	D	D	D	D	D	D	D

Option 2:
Example – Three control blocks, Five all-data blocks

aaa, bbb, ddd = original rows of control blocks

cccc = 4 bit encodings of control block types

X X X X X X X = per format of 64B/66B control block types

1

	1	2	3	4	5	6	7	8
1	1aaacccc	X	X	X	X	X	X	X
2	1bbbcccc	X	X	X	X	X	X	X
3	0dddcccc	X	X	X	X	X	X	X
4	D	D	D	D	D	D	D	D
5	D	D	D	D	D	D	D	D
6	D	D	D	D	D	D	D	D
7	D	D	D	D	D	D	D	D
8	D	D	D	D	D	D	D	D

Option 2:
Economical Linecode – Finishing touches

- The 512-bit/513-bit coding uses 0.1953125% of the allowable 0.36425% overhead
- Combine 8 (or 8n) 513-bit blocks into a 513 (or 513n) byte super-block to have an integral number of bytes
- Scrambling to ensure sufficient transitions and timing recovery
- Some sort of framing (perhaps at the super-block level) to recover the start of frame

Option 3:
Combination of lower MAC/PLS rate & more economical PCS

PCS-encoded line rate <40.149716 Gb/s
EXAMPLE:

Possible MAC/PLS rate	**39.5 Gbit/s**
+100 ppm	**39.50395 Gbit/s**
With 64B/65B coding	**40.121199**
Other tradeoffs between MAC/PLS rate and coding are possible	

Option 4:
Saving bits by not preserving preamble or IFG in PCS

Average MAC SDU size	Bitrate without preamble and IFG	With 64B/66B PCS
46 bytes (minimum)	30.476 Gb/s	**31.428 Gb/s**
100 bytes	34.203 Gb/s	**35.272 Gb/s**
500 bytes	38.513 Gb/s	**39.716 Gb/s**
1500 bytes (maximum basic)	39.479 Gb/s	**40.714 Gb/s**
2000 bytes (802.3as encapsulation)	39.607 Gb/s	**40.845 Gb/s**
9600 bytes (typical jumbo)	39.917 Gb/s	**41.164 Gb/s**
19900 bytes (maximum jumbo)	39.960 Gb/s	**41.209 Gb/s**

Not possible to fit within 40.149716 Gb/s payload of ODU3 by only eliminating preamble and IFG

Conclusions

- Specification of ~40Gb/s Ethernet compatible with existing OTN transport by selecting a MAC rate of 38.9 Gbit/s or less is feasible
- Specification of 40 Gb/s Ethernet compatible with existing OTN transport by specifying a linecode that requires less than 0.36425% of overhead is feasible
- Compatibility with existing OTN transport cannot be achieved with a MAC rate of 40.000 Gbit/s and 64B/66B coding by dropping ONLY preamble and IFG, but this COULD be considered in combination with other approaches to achieve the necessary fit.
- The objective proposed in Geneva has a good wording, as it permits choosing a solution from among all of the feasible approaches:

Support a speed of ~40 Gb/s at the MAC/PLS service interface while ensuring compatibility with OTN infrastructure