Technical & Economic Feasibility of 10km SMF 100GE Transceivers

IEEE 802.3 Higher Speed Study Group

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Outline

- Applicable HSSG Fiber Optic Ad Hoc SMF study alternatives
- 10km SMF 100GE Transceiver Technical Feasibility check list
- Gen1 100GE System Architecture
- Gen1 10km SMF 100GE Transceiver Architecture
- Gen1 10km SMF 100GE Transceiver Optical Performance
- Gen1 10km SMF 100GE Thermal Performance
- Gen1 10km SMF 100GE Transceiver Economic Feasibility
- Gen2 100GE System Architecture
- Gen2 10km SMF 100GE Transceiver Architecture
- Gen2 10km SMF 100GE Transceiver Technology Alternatives
- Gen2 10km SMF 100GE Transceiver Economic Feasibility
- Discussion

Reach (Technical) Feasibility of 100GE alternatives

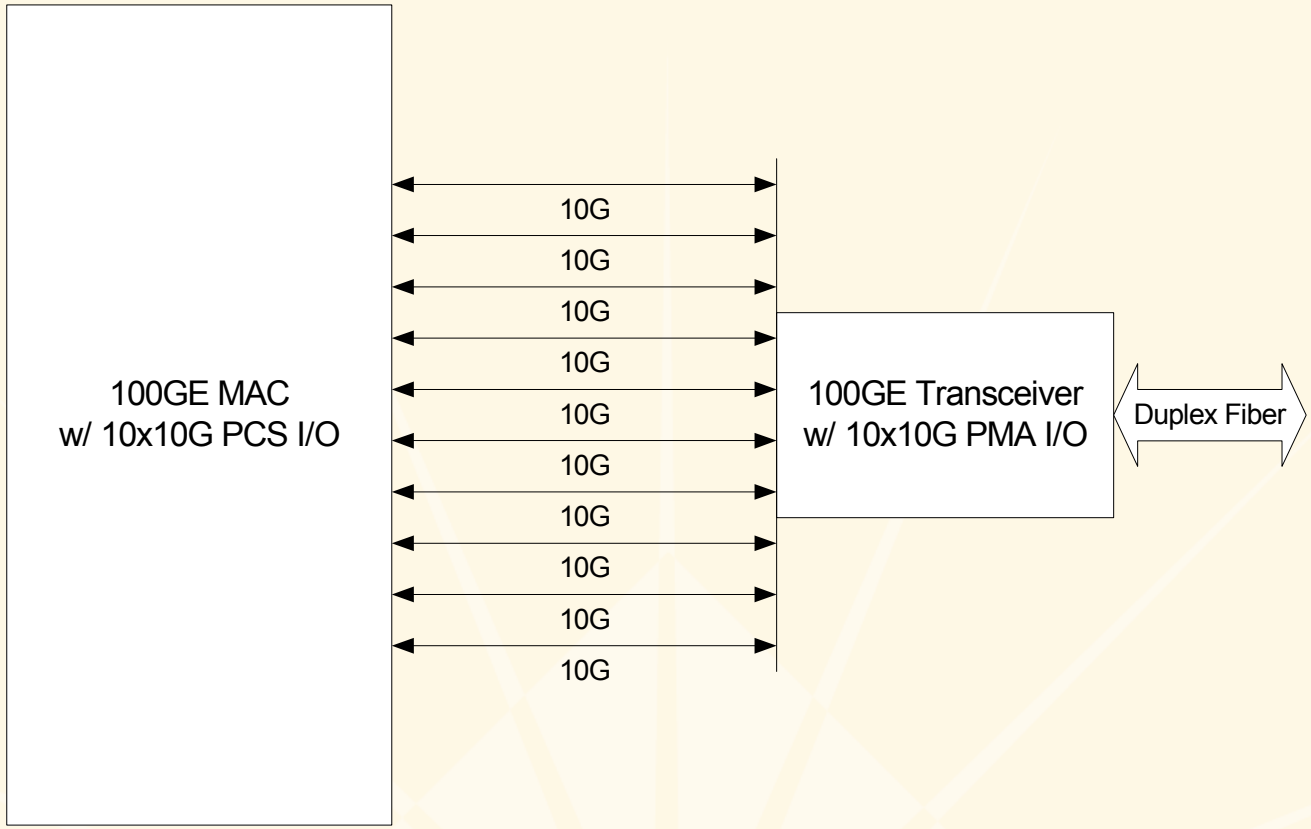
SMF	10km 1310nm	40km 1310nm	10km 1550nm	40km 1550nm
10x10G DML	yes (10λ span can not be un-cooled)	yes (need new DML, RX APD or SOA)	yes (need new DML)	maybe (need new DML, RX APD or SOA)
10x10G ML	yes	yes (need RX APD or SOA)	yes	yes (need RX APD or SOA)
5x20G / 4x25G DML	yes (need new DML)	maybe (need new DML & RX SOA)	maybe (need new DML)	no
5x20G / 4x25G ML	yes (need new EML)	yes (need new EML & RX SOA)	yes	yes (need RX DC)
2x50G DQPSK ML	yes (need I/Q ML)	yes (need I/Q ML & RX DC & OA)	yes (need I/Q ML & RX DC)	yes (need I/Q ML & RX DC)
1x100G TDM ML	yes (need new ML & maybe RX DC)	yes (need new ML & RX DC & OA)	yes (need new ML & RX DC (& OA?))	yes (need new ML & RX DC (& OA?))

Green shading designates alternatives under detailed study by Fiber Optic Ad Hoc contributors.
Red oval designates alternative which is the subject of this presentation.

10km 4x25G EML Transceiver Technical Feasibility

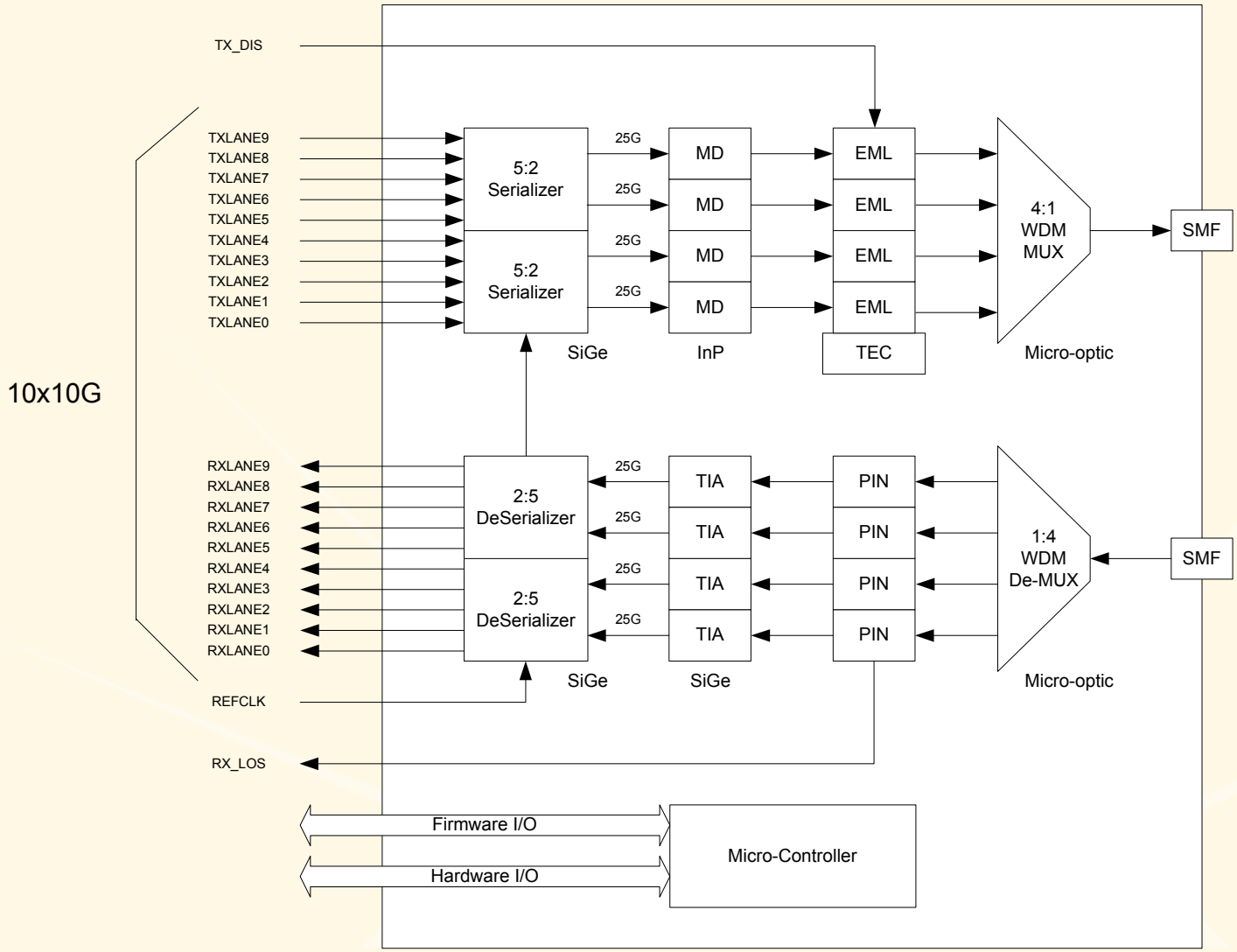
Item	Status	Comments
Optical Link Budget	√	10km cooled EML based link budget shown. Updated link budget in this presentation.
Dual 5:2 SiGe SerDes	√	40G SiGe SerDes commercially available. Additional 20G data in this presentation.
Quad InP Mod Driver	√	40G InP MDs commercially available. Additional 20G data in this presentation.
Quad EML TOSA w/ WDM Mux	√	40G EMLs commercially available. Additional 20G data in this presentation. Mux micro-optics commercially available.
Quad PIN/TIA ROSA w/ WDM DeMux	√	40G PIN/TIAs commercially available. Additional 20G data in this presentation. DeMux micro-optics commercially available.
Connector / I/O Signal Integrity	√	Enhanced PT20 SMT Connector available. 10G signal integrity shown.
Mechanical / Thermal	√	Viable mechanical form factor shown. Updated Transceiver power, and thermal data in this presentation.

Gen1 100GE System Architecture



- PCS in the MAC performs skew alignment and lane re-ordering.
- An alternate architecture uses 12x10G PCS - PMA I/O.

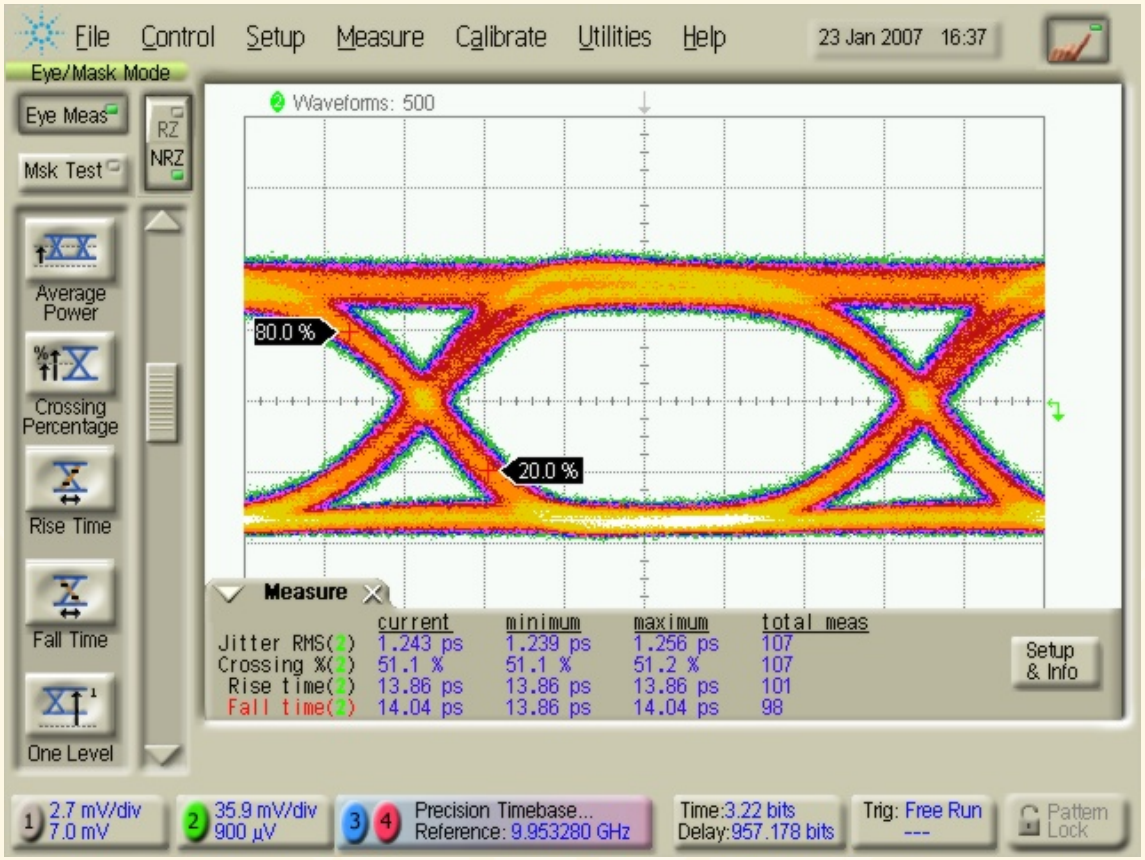
Gen1 10km 4x25G EML Transceiver Architecture



10km 4x25G EML 100GE Transceiver Optical Link

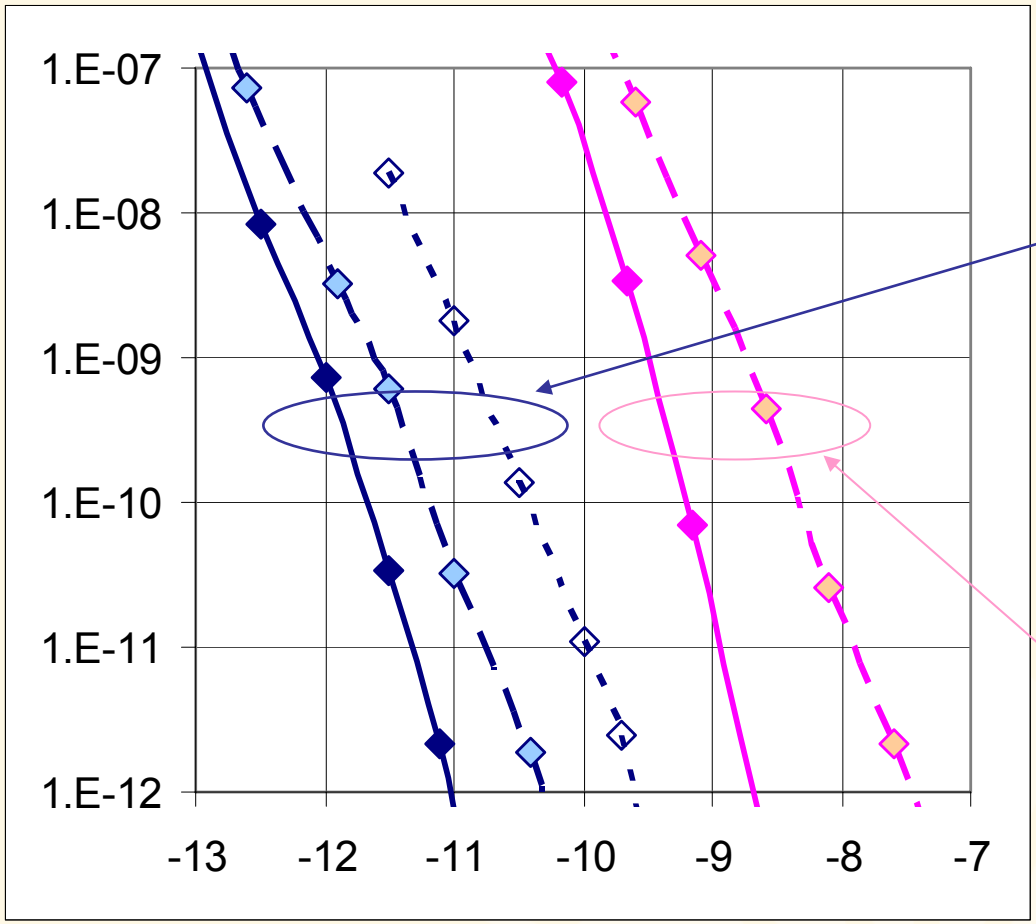
- Example 1310nm TP2 to TP3 per λ 10km 6dB link budget
  - Max output power: 2.0dBm
  - Min output power: -2dBm
  - Min receiver sensitivity: -10dBm
  - Max penalties: 2dB
  - Max loss (4dB fiber + 2dB other losses): 6dB
- Some considerations for a 10km WDM standard:
  - E.R. that supports DML alternatives
  - Output power that supports EML alternatives
  - Ability to trade-off TDP versus output power
  - Losses through variety of optical Muxes and DeMuxes
  - Wavelength spacing without stringent stability requirements
  - Wavelength span consistent with good monolithic laser (CW or DM) array yield in a variety of processes.

20G Transmitter Performance



- 25G un-cooled 1328nm EML Transmitter
- 20G PRBS 2^31-1 data, 75^{o} C case temperature
- EML TOSA provided by Milind Gokhale, Apogee Photonics

20G Receiver Performance



20G curves: PRBS 2^31-1

- 25G un-cooled 1328nm EML Transmitter →
- 0km, 10km, 20km SMF-28 →
- 40G PIN/TIA Receiver (sub-optimal 20G sampling phase due to CDR designed for 40G operation.)

40G curves: PRBS 2^31-1

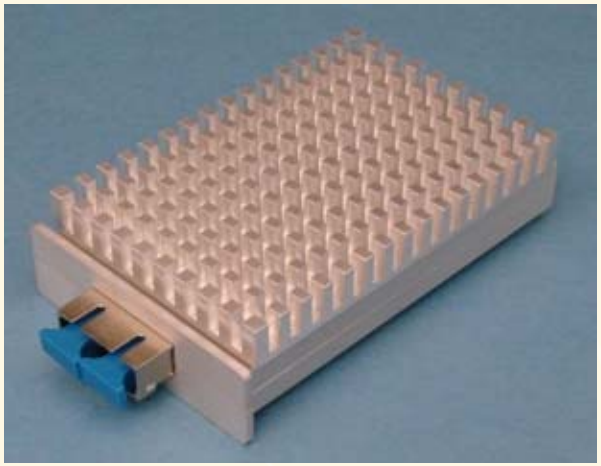
- 40G cooled 1550nm EML Transmitter →
- 0km, 2.4km SMF-28 →
- 40G PIN/TIA Receiver

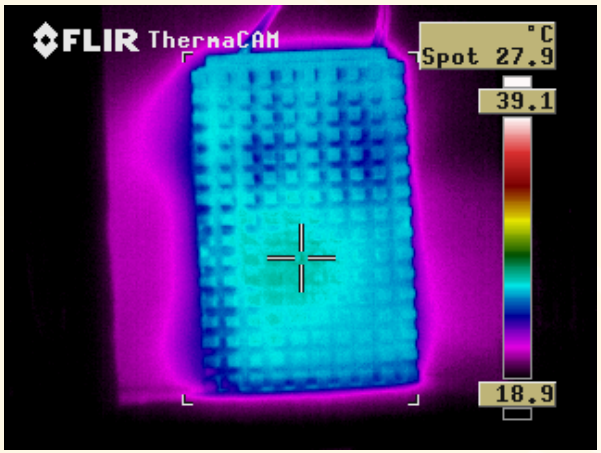
Data: Tedros Tsegaye, Yuri Vandyshev, Finisar Corp.

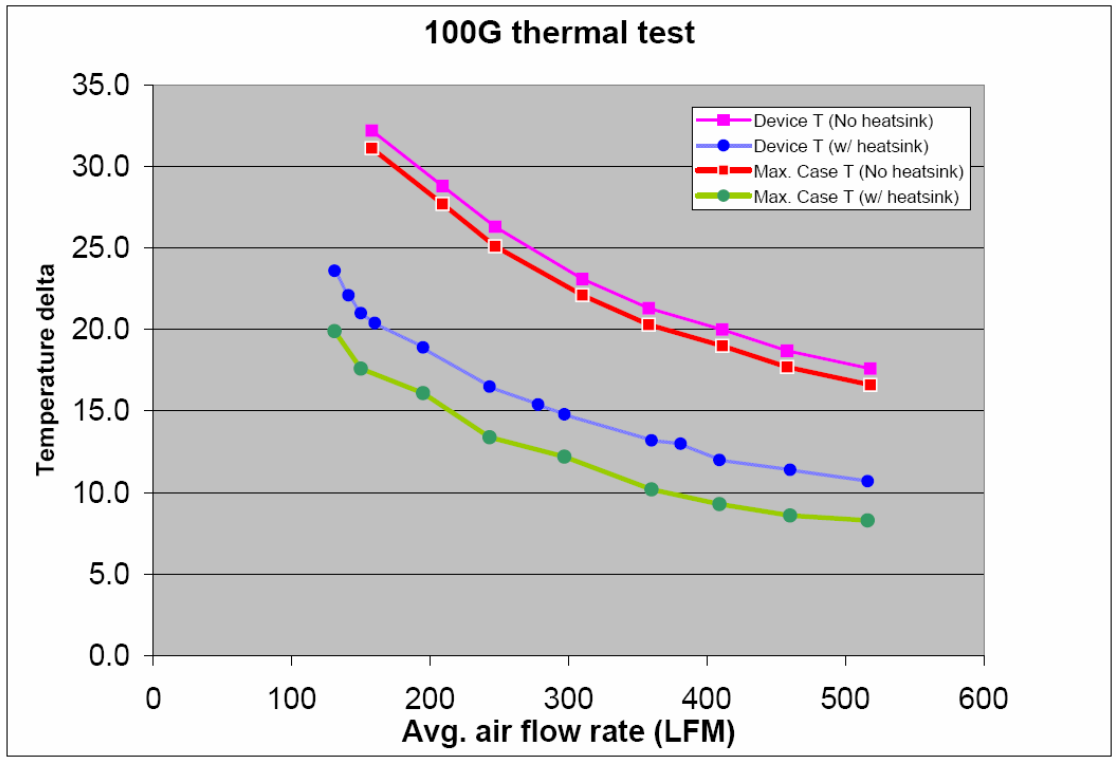
Gen1 10km 4x25G EML Transceiver Power

10GE-ER XENPAK Component	Power Watts	10km 4x25G Transceiver Component	Power Watts
XAUI (SiGe)	2.2	Dual 5:2 SerDes (SiGe)	6.5
Mod Driver (InP)	0.5	Quad MD (InP)	2.0
EML + TEC TOSA	1.5	Quad EML + TEC TOSA w/ WDM micro-optic Mux	4.5
PIN/TIA ROSA	0.3	Quad PIN/TIA ROSA w/ WDM micro-optic DeMux	1.2
other ICs	0.3	other ICs	0.5
Maximum operating power	**~5**	**Maximum operating power**	**~15**

100GE Transceiver Thermal Measurements







- Temperature delta (20W load) = T measured – T air
- Device T from thermocouple on “OSA” (10W load)
- Max. Case T from IR camera image

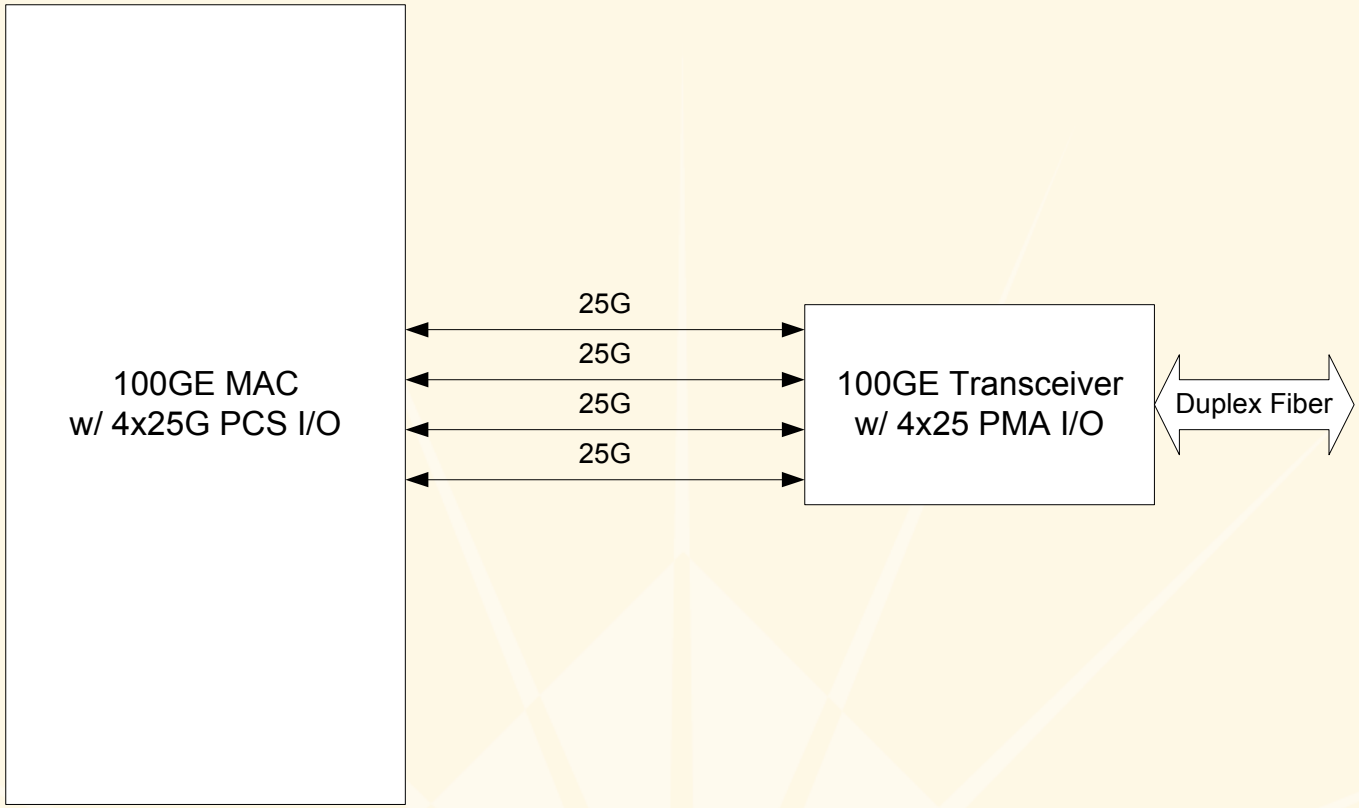
- Final mechanical and I/O specifications to be developed through industry MSA.
- Data: Daniel Kim, Finisar Corp.

Gen1 10km 4x25G Transceiver Economic Feasibility

10GE-ER XENPAK Component	Relative Cost	10km 4x25G Transceiver Component	Relative Cost
XAUI (SiGe)	1x	Dual 5:2 SerDes (SiGe)	3x
Mod Driver (InP)	1x	Quad MD (InP)	3x
EML + TEC TOSA	1x	Quad EML + TEC TOSA w/ WDM micro-optic Mux	4x
PIN/TIA ROSA	1x	Quad PIN/TIA ROSA w/ WDM micro-optic DeMux	4x
FR4 PCBA, XENPAK parts & PT20 connector	1x	Nelco PCBA, new form factor parts & connector	2x
Single channel testing	1x	Four channel parallel testing	1x
Weighted average	**1x**	**Weighted average at similar volumes and points in time**	**4x**

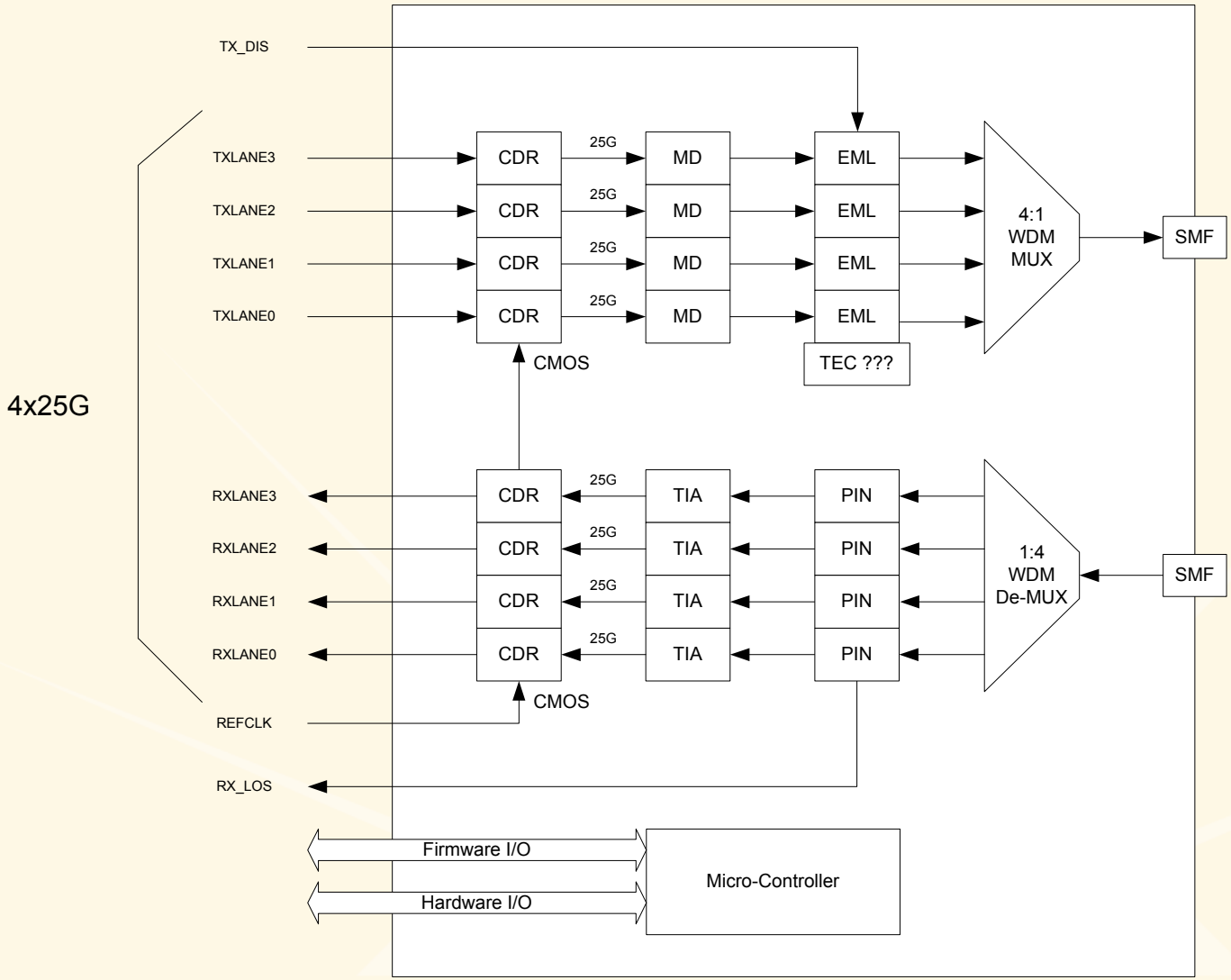
Amortization of development and test equipment costs not included.

Gen2 100GE System Architecture



- PCS in the MAC performs skew alignment. Lane re-ordering is not required.
- 25G I/O requires 45nm or 32nm CMOS process technology.
- A 10:4 SerDes IC can be used for interfacing with Gen1 MACs.

Gen2 10km 4x25G EML Transceiver Architecture



Gen2 100GE Transceiver Technology Alternatives

- It is too early to determine the best technology to reduce the size/cost/power of Gen2 100GE Transceivers, but there are many promising alternatives.
- Multiple Photonic Integrated Circuit (PIC) approaches are under investigation.

<u>Hybrid Si PIC approach</u>

- EML alternative
  - Si PIC with quad modulator, WDM Mux, and quad InP CW DFBs
  - Si modulators reported by Intel, SiOptical, Luxtera, Kotura, MIT, Cornell, UT Austin, UCLA, NTU IME, others
- DML alternative
  - Si PIC with output WDM multiplexer, and quad InP 25G DFBs
  - 20G or higher speed DFBs reported by Hitachi, Excelight, NEC, others

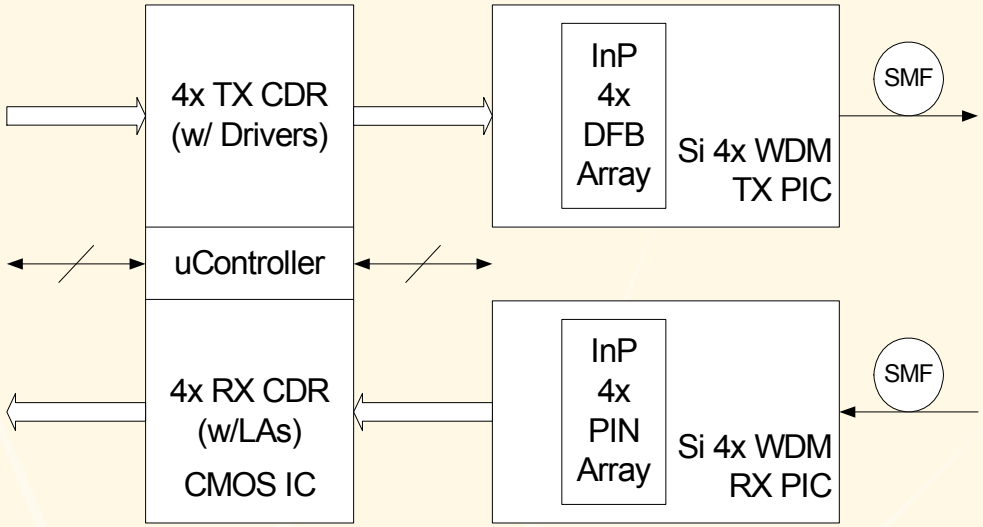
<u>Monolithic InP PIC approach</u>

- EML alternative
  - InP PIC with quad CW DFB array, quad modulator and WDM Mux
  - PICs reported by Infinera, CyOptics, others
- DML alternative
  - InP PIC with quad 25G DFB array and WDM Mux

Gen2 100GE Transceiver P/IC Partitioning Alternatives

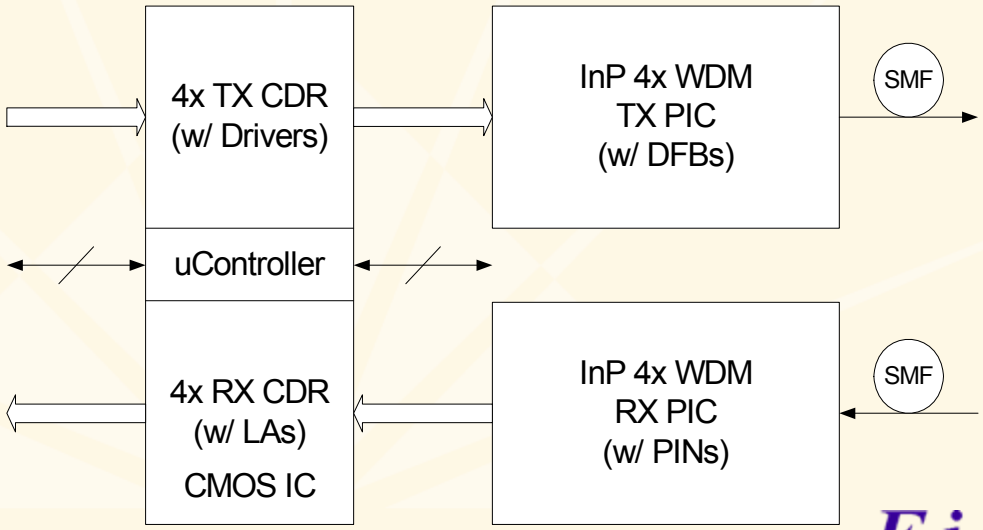
Hybrid Si PICs

- CW or 25G DFBs
- Flip-chip InP Arrays
- Si PIC 25G Drivers & TIAs (or separate)
- 1 CMOS ASIC
- Multiple packaging alternatives



Monolithic InP PICs

- CW or 25G DFBs
- InP PIC 25G Drivers & TIAs (or separate)
- 1 CMOS ASIC
- Multiple packaging alternatives



Gen2 10km 4x25G Transceiver Economic Feasibility

10GE-LR XFP Component	Relative Cost	10km 4x25G Transceiver Component	Relative Cost
Bi-directional CDR w/ µController (CMOS)	1x	Quad bi-directional CDR w/ µController (CMOS)	3x
Mod Driver (SiGe)	1x	Quad MD (if separate: 3x cost)	0x
DFB TOSA	1x	Quad 25G WDM Mux PIC TOSA w 4x MDs	5x
PIN/TIA ROSA	1x	Quad 25G WDM DeMux PIC ROSA w/ 4x TIAs	5x
FR4 PCBA, XFP parts & PT20 connector	1x	Nelco PCBA, new form factor parts & connector	2x
Single channel testing	1x	Four channel parallel testing	1x
Weighted average	**1x**	**Weighted average at similar volumes and points in time**	**5x**

4x25G Transceiver cost is dominated by PIC yield assumptions.

Discussion

Gen1

- Technical Feasibility of a Gen1 10km SMF 100GE Transceiver alternative shown.
- Economic Feasibility of Gen1 Transceiver alternative for core switching applications shown.
- Gen1 development cycle is approximately 2 to 3 years.

Gen2

- Technical Feasibility alternatives for Gen2 10km SMF 100GE Transceiver outlined.
- Economic Feasibility of Gen2 Transceiver alternatives for distribution switching outlined.
- Gen2 development cycle is approximately 5 to 6 years.

Long Term Gen2

- Economic Feasibility of Gen2 Transceivers for access switching will result from volume driven cost reductions.
- Process yield improvements (cost reduction) will take multiple years.
- The quickest path to low cost, high volume 100GE is to define a standard so that many focused development efforts take place.