25Gbps SerDes

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Outline

- Introduction
- 25G SerDes Design Considerations
  - Different signaling schemes
  - Equalization
  - Crosstalk cancellation
  - FEC
  - Analog/digital partition
- Simulation Results
- Conclusions

Introduction

In 100Gbps Ethernet backplane, replace XFI with:

25Gbps SerDes

Advantage: Higher density

OIF CEI-25G is work in progress

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  - Equalization
  - Crosstalk cancellation
  - FEC
  - Analog/digital partition
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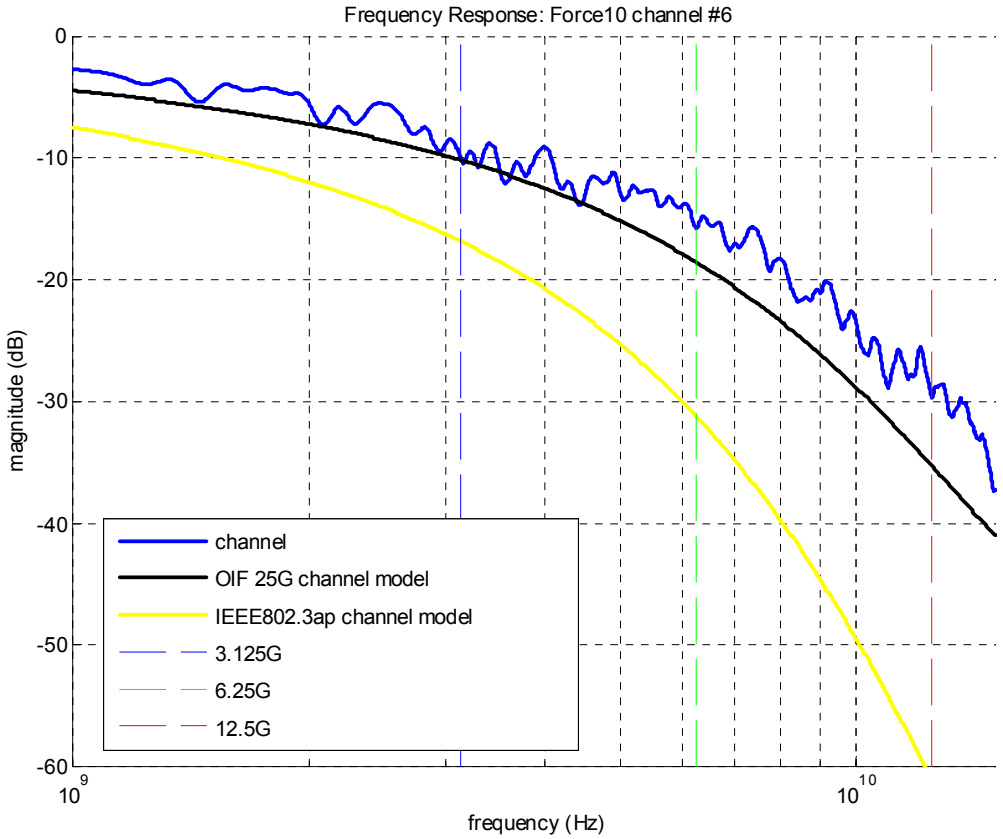
Signaling/modulation Choices

- NRZ is the choice of 10G BASE-KR and OIF CEI-11G.
  - Large installed base
  - People want to use NRZ in 25G as long as it is feasible
- PAM4
- Constant envelope modulations: QPSK, DQPSK,FSK…
- OFDM
- Partial-response signals: Duo Binary, PR4

The Benefit of Higher-order Modulation

Note: the OIF 25G mask is updated based on the Q107 meeting



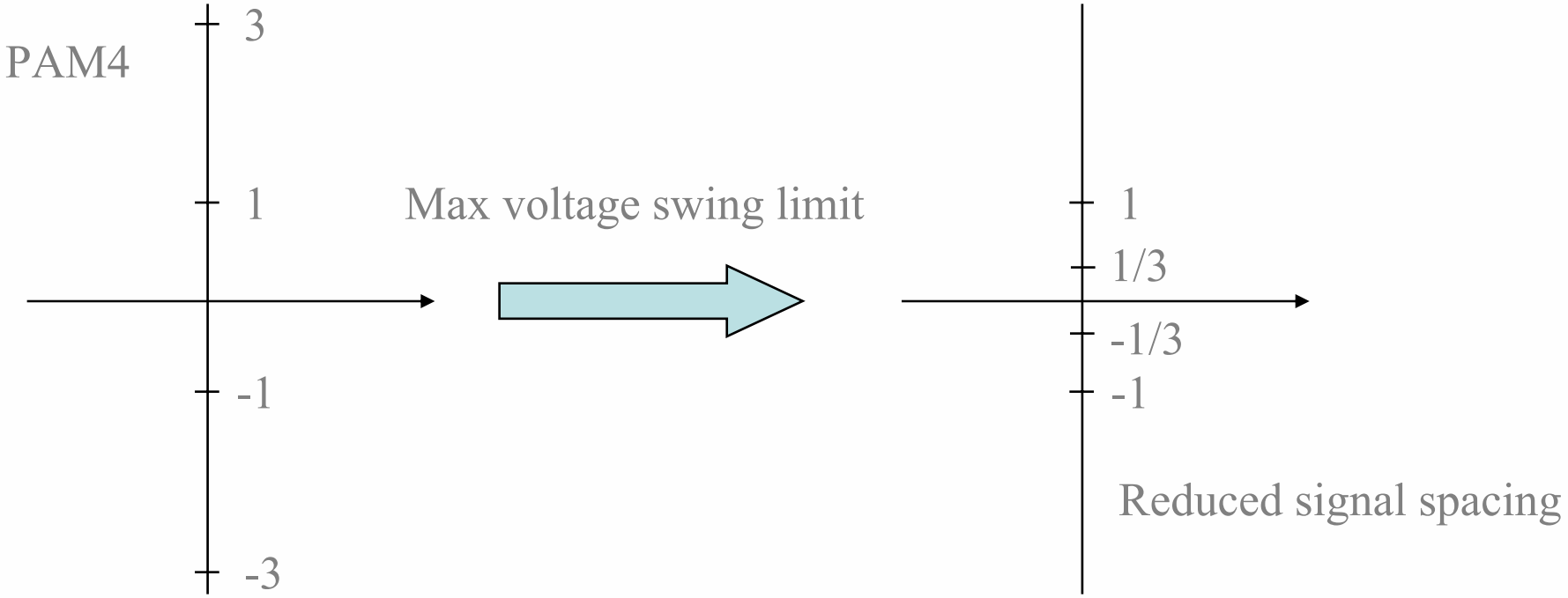
NRZ v.s. PAM4/QPSK

Data rate (Gbps)	12.5	25
½ symbol rate gain (dB)	**5**	**15**

The difference is larger at higher data rates.

Lower insertion loss at reduced symbol rate

The Drawback of Amplitude Modulation



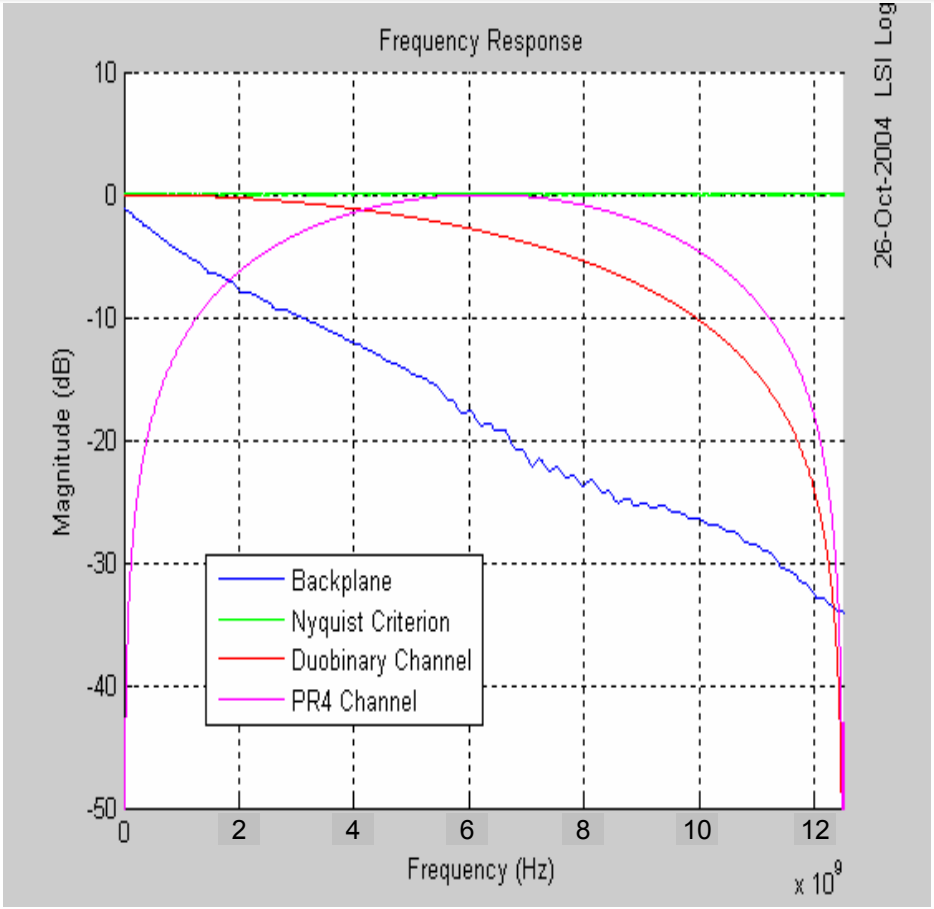
The 3x reduction in minimum distance results in 9.5 dB SNR loss.

Comparison between Modulation Schemes

Modulation	Symbol Rate	9.5dB loss	**Implementation**
NRZ	25G	N	**25GS/s ADC**
PAM4	12.5G	Y	**12.5GS/s ADC**
QPSK	**12.5G**	**N**	**12.5GS/s circuit** **Difficult to implement in DC**

- Analog implementation of QPSK requires a carrier frequency much higher than the data rate in order to maintain the orthogonality.
- OFDM/QPSK implemented in the digital domain can maintain the othogonality without using a carrier frequency.

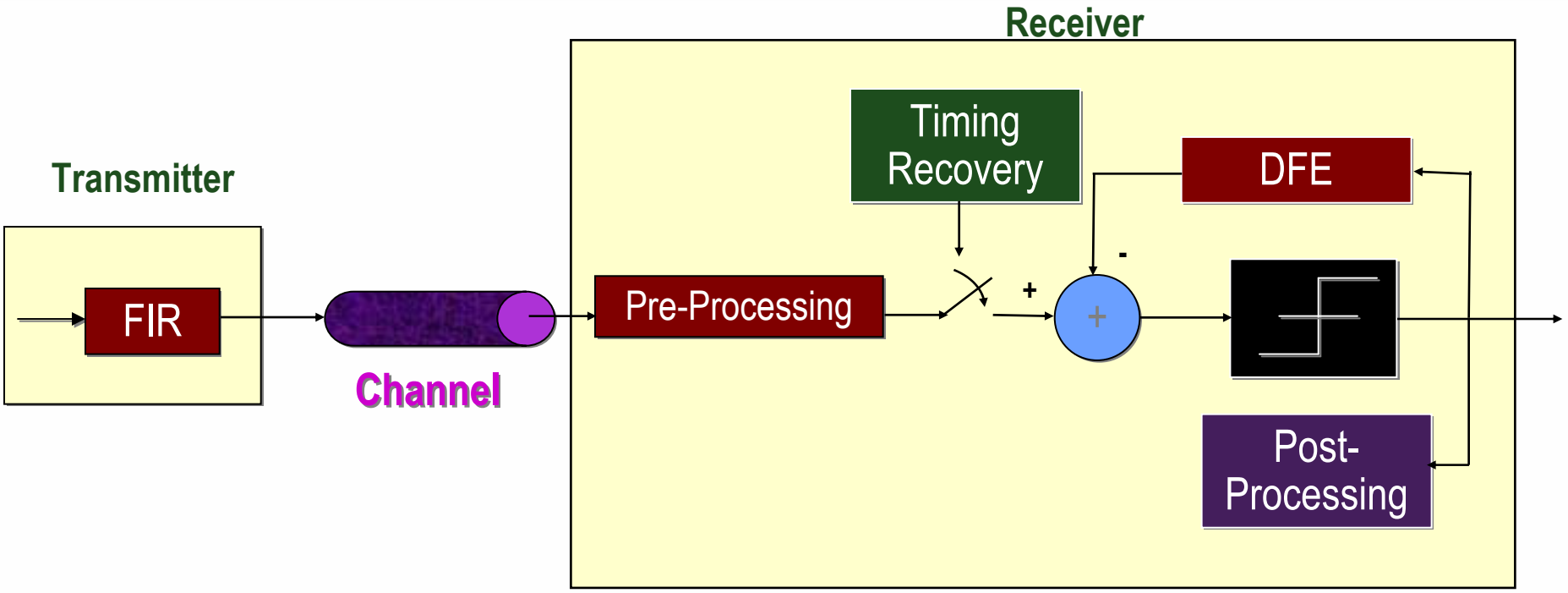
Partial-Response Signals



- Ideal NRZ equalization target is flat spectrum.
  - Requires a lot of high frequency boost.
- DB's 1+D equalization target has a null at the Nyquist frequency.
  - Better match to the channel at high frequencies and consequently requires less high frequency boost.
- PR4 has nulls at both DC and Nyquist.
  - Null at DC may match DC-null in AC coupled systems, but PR-4's DC null is much deeper.
  - Results in throwing away the signal in the low frequency range where the SNR is strongest.

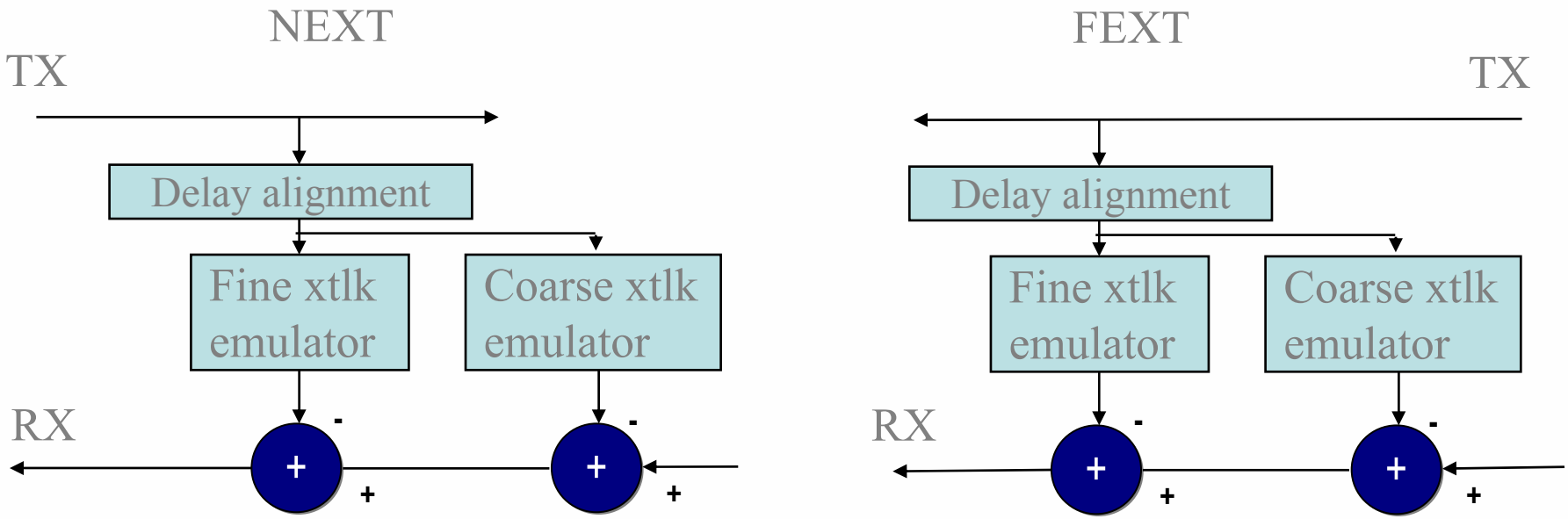
- Change of equalization target by relaxing the zero-ISI condition
- ML sequence detection is needed for optimal detection

Equalization



- Traditional DFE is not enough.
- Super DFE employs both front-end and back-end signal processing to handle ISI in a more intelligent way.
- Super DFE can have performance similar to that of a 40-tap DFE, but with much fewer taps.

Crosstalk Cancellation

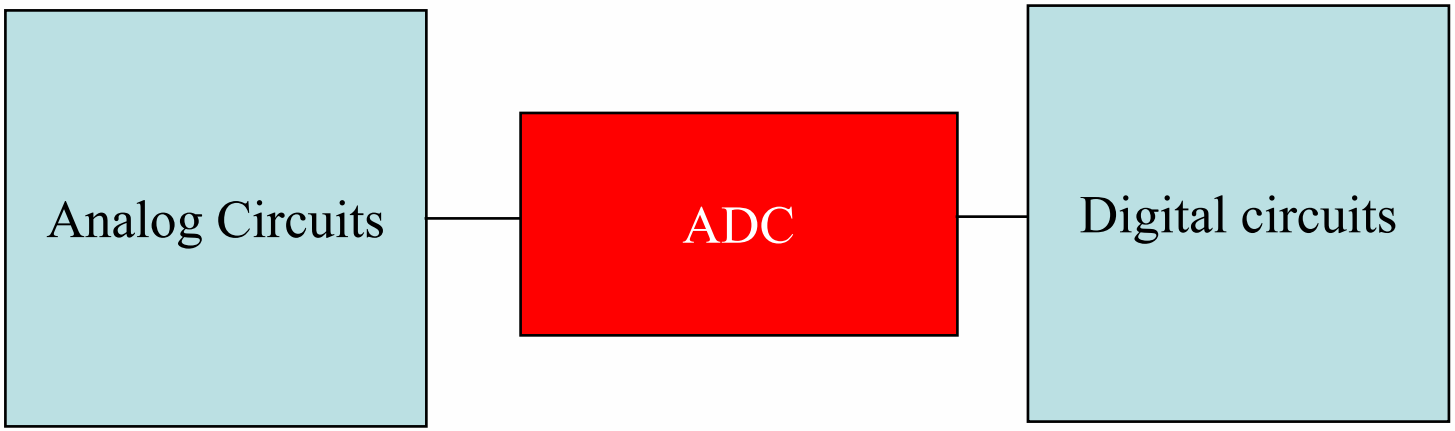


- Emulate NEXT or FEXT at the receiver
- Cancel both NEXT and FEXT
- Do-able for 4-lane Ethernet SerDes

Error Control

- Error propagation is more severe at 25G, so burst correcting code is a must.
  - (2112,2080) shortened code was adopted by IEEE 802.3ap.
  - (1584,1560) Fire code is used by OIF CEI.
- Implementation considerations
  - Parallel decoder
  - Small number of parity bits
  - (2112,2080) code has only 32 bits OH and requires circuits running at only 769.2MHz if used in 25G.

Analog/Digital Partition



- Traditional SerDes is mainly an analog design.
- Some building blocks (DFE, CDR) can be moved to the digital domain for process portability and design scalability.
  - Digital DFE: 20-tap DFE is do-able
- More digital signal processing can be introduced to handle the challenging 25G channels.
  - OFDM/QPSK
  - Soft decision Viterbi decoder
- Low power GS/s ADC is the key: 4-6 bits ADC with 100mW power consumption is feasible.

Outline

- Introduction
- 25G SerDes Design Considerations
- Simulation Results
  - Model description
  - Channel frequency responses
  - Impact of crosstalk cancellation
  - Comparison between different signaling schemes
  - Effect of smarter equalization
  - Performance with better channel materials
  - Reduced data rate
- Conclusions

Simulation - Analytic Model

- Analytic model is used to get slicer SNR at optimal sampling point.
  - Includes
    - Intersymbol Interference (channel and package)
    - Random Jitter
    - Electronics (White) Noise
    - Crosstalk (NEXT and FEXT)
    - Duty Cycle Distortion
  - Does Not Include
    - Receiver Sensitivity
    - Other Sources of DJ

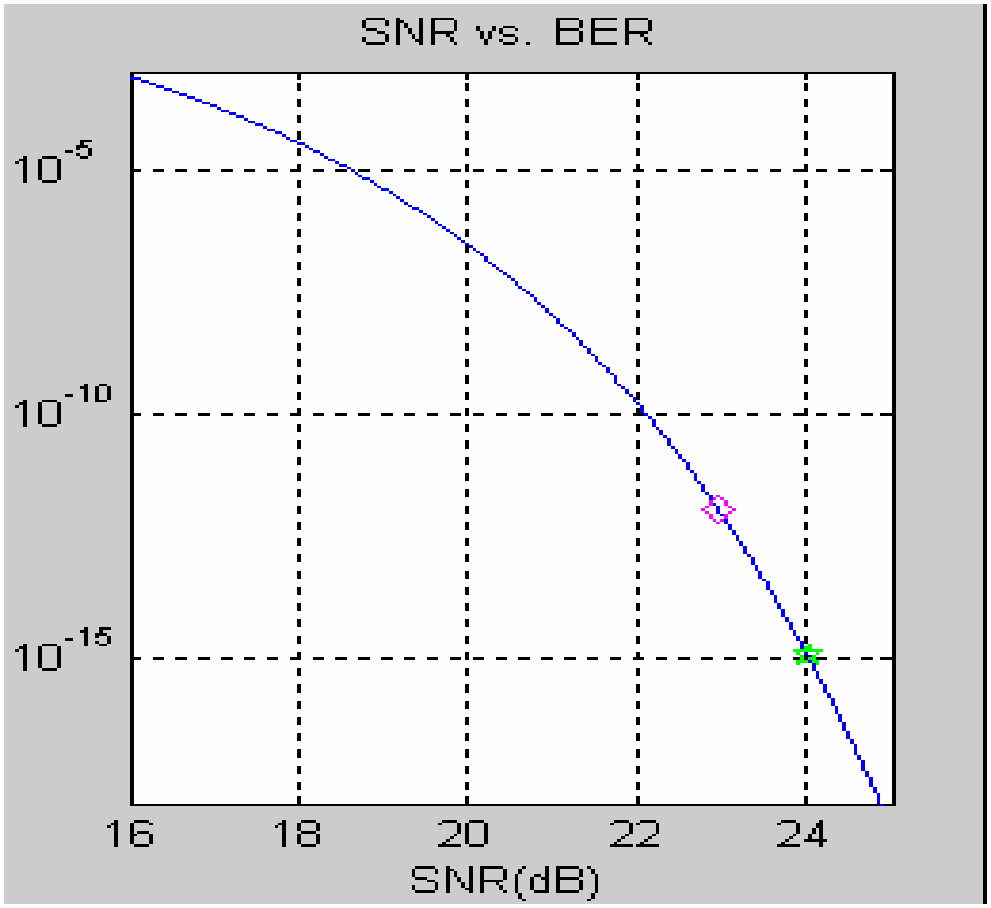
Reference: J.Caroselli and C. Liu, "An Analytic System Model for High Speed Interconnects and its Application to the Specification of Signaling and Equalization Architectures for 10Gbps Backplane Communication", DesignCon 06.

Required SNR

$$SNR = \frac{d_{\min}^2}{\sigma^2}$$

$$\Pr_{err} \approx \frac{1}{2} erfc\left(\frac{\sqrt{SNR}}{2\sqrt{2}}\right)$$

Approximately 24dB is required for an error rate of 10^{-15} and 23 dB for 10^{-12}.

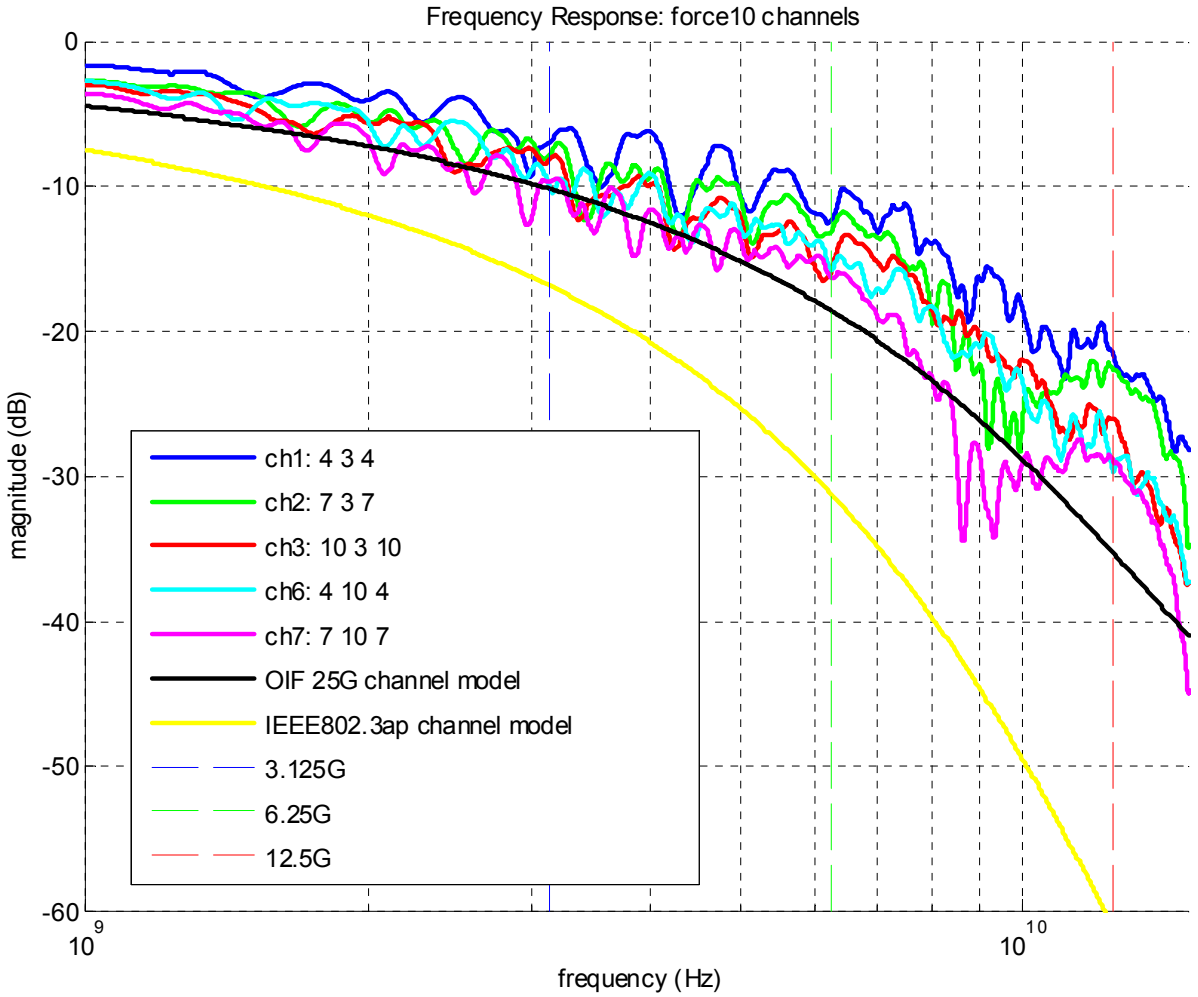


Simulation Overview

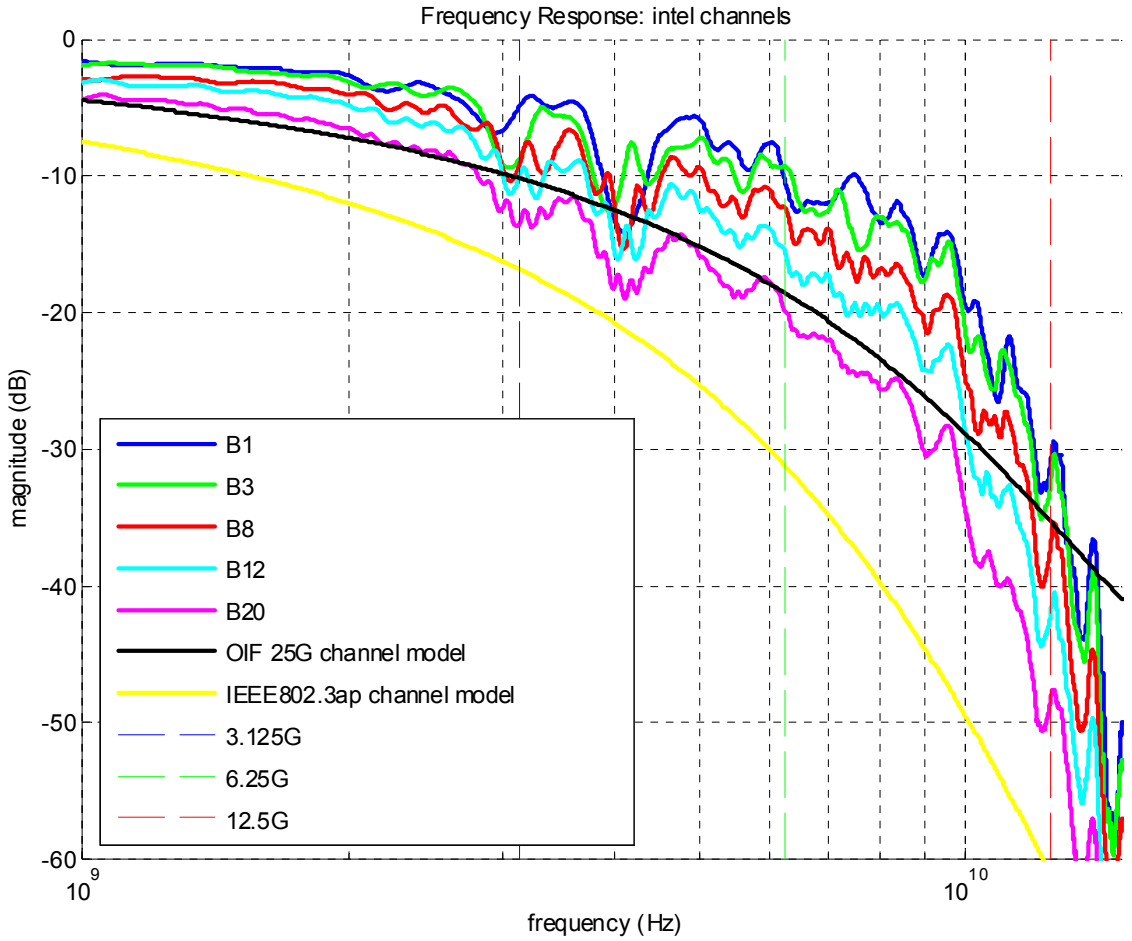
- Different Signaling and Equalization architectures are compared.
- The number of taps in the feed forward and feedback equalizers are varied.
- All tap values are ideal.
- The effect of one (worst case) near-end crosstalk aggressor is considered.
- A simple RC model with pole at 0.75*baud rate is used for the transmitter.
- IEEE802.3ap capacitor-like package model included on both transmitter and receiver.

Data rate	25 Gb/s
Electronic noise	40dB
Random Jitter	1ps sigma
TX/RX Package	Added
Cross Talk	See noted

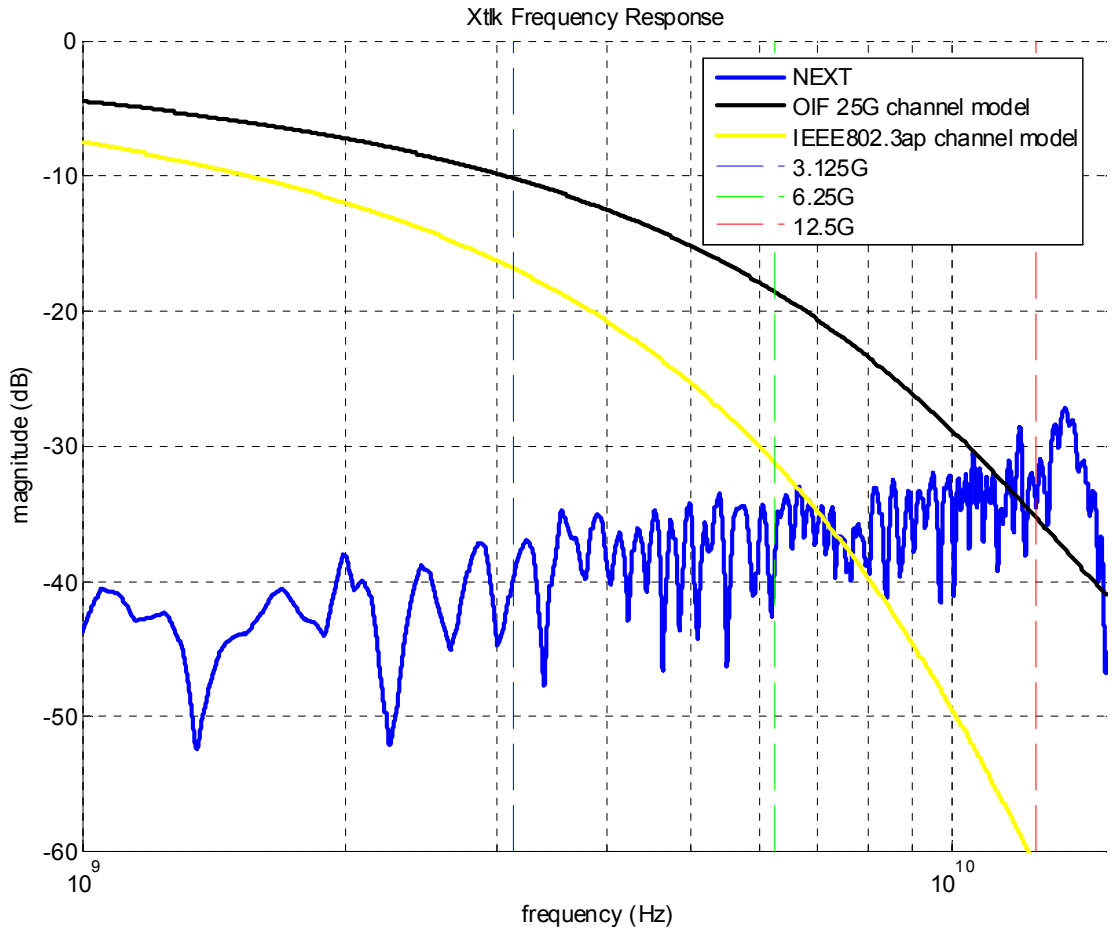
Force10 Network Channels



Intel Channels



NEXT



- Modest crosstalk
- Magnitude above signal mask at 12.5G

The Impact of Crosstalk Cancellation

With modest crosstalk

- All with 3-tap TX FIR.
- Number of DFE taps required to achieve BER of 10-15

Force10 Channels	NRZ	DB	**PAM4**
1	85	60	**42**
3	>>100	>>100	**100**
7	>>100	>>100	**>>100**

If crosstalk is cancelled

Force10 Channels	NRZ	DB	**PAM4**
1	37	39	**20**
3	28	29	**21**
7	67	72	**47**

Note: DB is better than NRZ with crosstalk,
but when crosstalk is perfectly cancelled, the advantage of DB (easier equalizer target and less boost) is gone

Comparison between Signaling Formats

- All with 3-tap FIR and cross talk cancellation.
- Number of DFE taps required to achieve BER of 10^{-15} :

Channels	NRZ	DB	PAM4	QPSK
Intel B1	29	28	17	8
Intel B3	41	41	19	8
Intel B8	39	40	42	7
Intel B12	34	40	34	7
Intel B20	80	90	19	7
Force10 1	37	39	20	5
Force10 2	40	45	30	5
Force10 3	28	29	21	4
Force10 6	48	48	38	4
Force10 7	67	72	47	5

PAM4 has better performance than NRZ.

Results with Super DFE

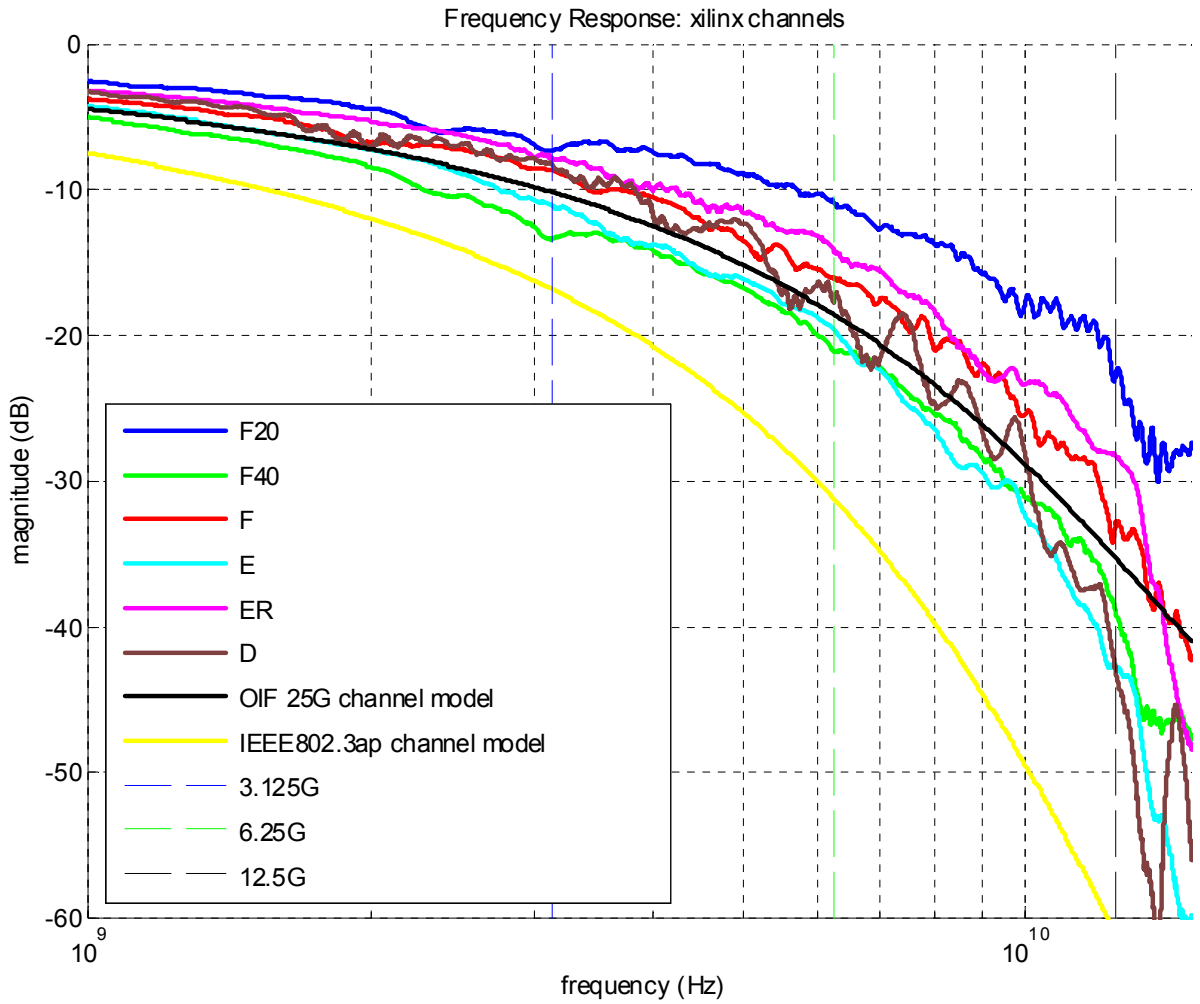
6-tap FIR and 20-tap DFE, NRZ signaling, crosstalk cancellation

Channels	DFE	**Super DFE**
Intel B1	22.48	**24.34**
Intel B3	21.01	**24.73**
Intel B8	21.68	**24.36**
Intel B12	21.45	**24.64**
Intel B20	19.67	**24.72**
Force10 1	23.41	**26.39**
Force10 2	22.75	**24.19**
Force10 3	23.36	**27.42**
Force10 6	23.69	**26.48**
Force10 7	21.58	**23.18**

Only 20-tap DFE is needed for NRZ.

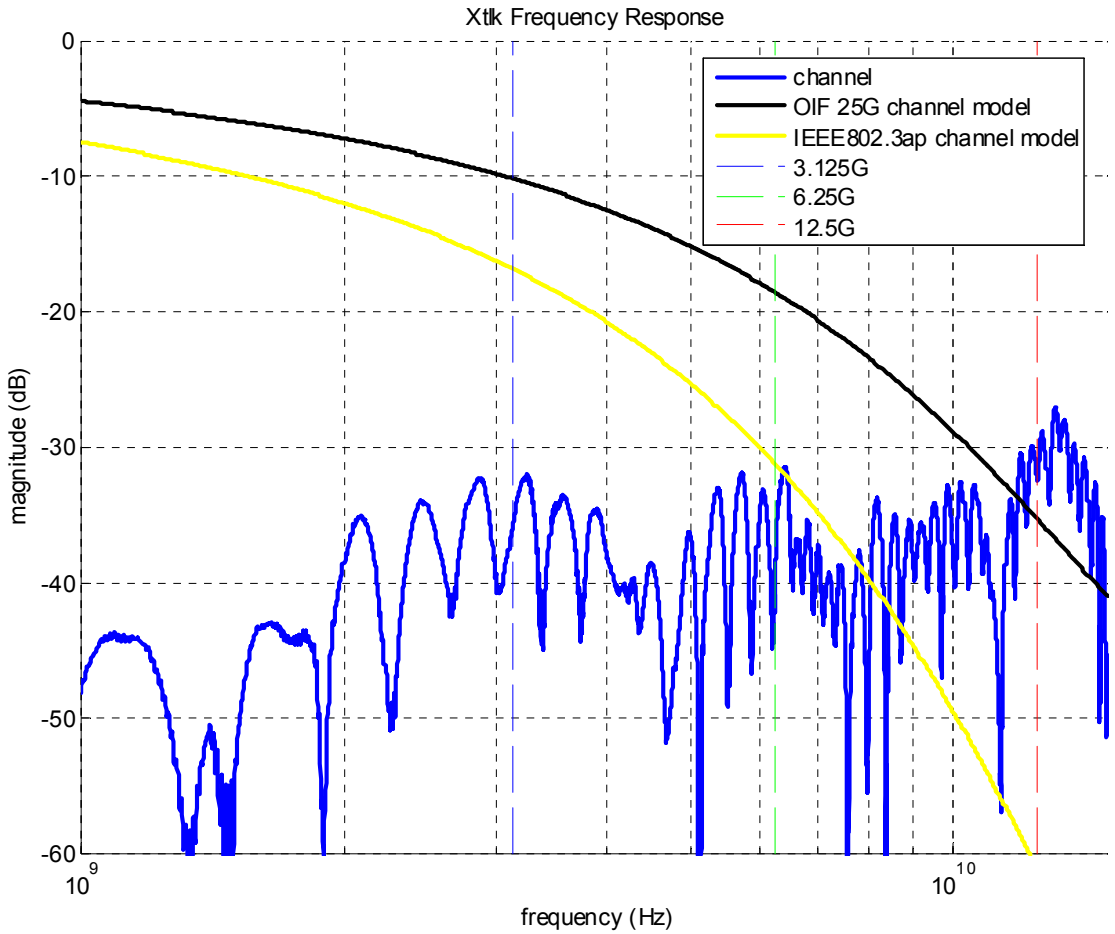
(PAM4 needs slightly fewer taps: 15-tap for B8, 20-tap for ch2)

Xilinx Channels



Backplane material: Rogers Hybrid

F20 NEXT


Xtlk Frequency Response
channel
OIF 25G channel model
IEEE802.3ap channel model
3.125G
6.25G
12.5G
magnitude (dB)
frequency (Hz)
0
-10
-20
-30
-40
-50
-60
10^9
10^10

System Tradeoff

NRZ signaling, 8-tap DFE
Crosstalk cancellation

Xilinx Channels	SNR: DFE (dB)	**SNR: super DFE (dB)**
F20 (20”)	29.01	**29.01**
ER (27”)	22.92	**28.78**
F (34”)	19.74	**25.91**

Backplane material: Rogers Hybrid

Channels	Raw materials	Overall system	**# of Lanes**
Rogers v.s. FR4	70-80% higher cost	15% higher cost	**40%**

Does it make sense to use better materials for 25G?

Reduced Data Rate

At 22Gbps, 6-tap FIR and super DFE, NRZ signaling, crosstalk cancellation

Number of taps needed to have a BER of 10^{-15}:

Channels	**Super DFE**
Intel B3	**12**
Intel B8	**10**
Intel B20	**13**

Summary of Simulation Results

- Crosstalk cancellation is essential.
- Higher order modulation provides better performance.
- Intelligent equalization technique can support NRZ with a DFE of only 20 taps.
- To use a DFE with less than 10 taps
  - Better channel materials
  - QPSK
  - 22Gbps or BER of 10^{-12}

Conclusions

- The support of 25G SerDes over backplanes at higher speed demonstrates system feasibility for 100G based systems.
- A combination of signaling formats, equalization scheme, crosstalk cancellation, FEC and analog/digital partition can make 25G SerDes feasible.