Nx10G Electrical I/O Issues

IEEE 802.3 Higher Speed Study Group

12-15 November 2007

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Outline

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  - 100GE
  - 2x40GE
  - 10x10GE
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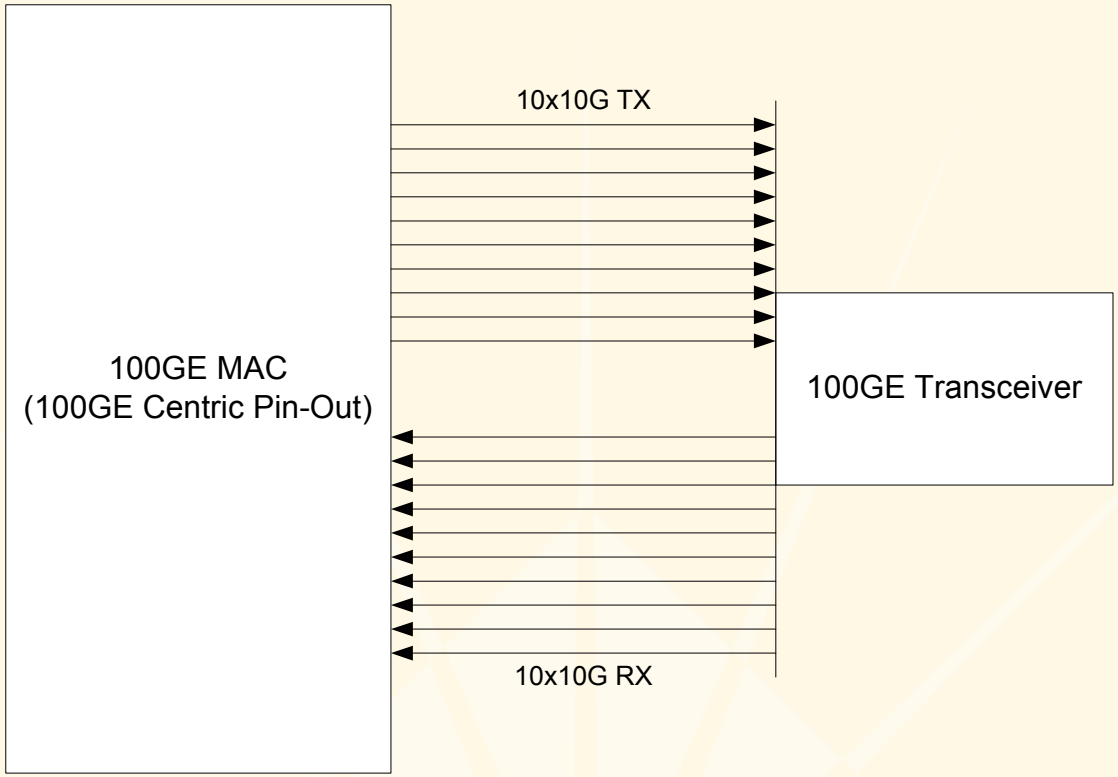
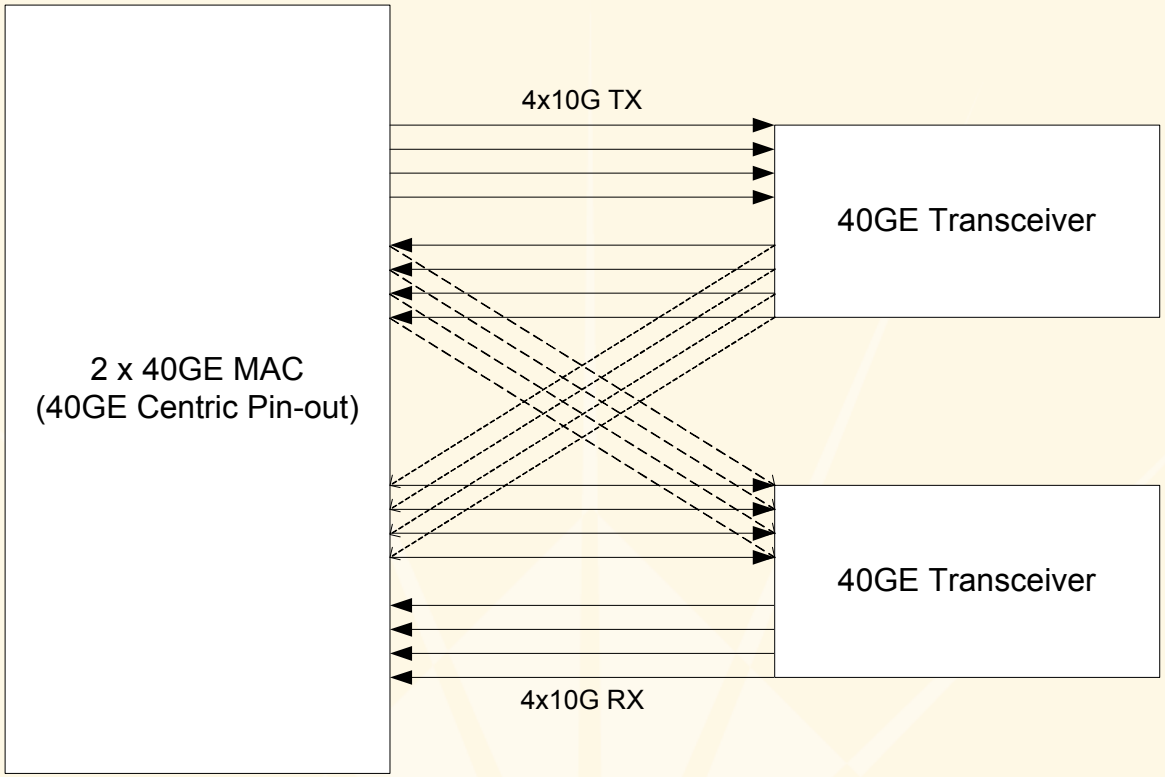
- 10G Jitter Budget
  - Single Channel Model
  - Proposal Comparison
  - Discussion
  - RX Equalizer Considerations
- 10G Lane Encoding
  - Discussion
- Summary

10G Lane Ordering: 100GE Mode



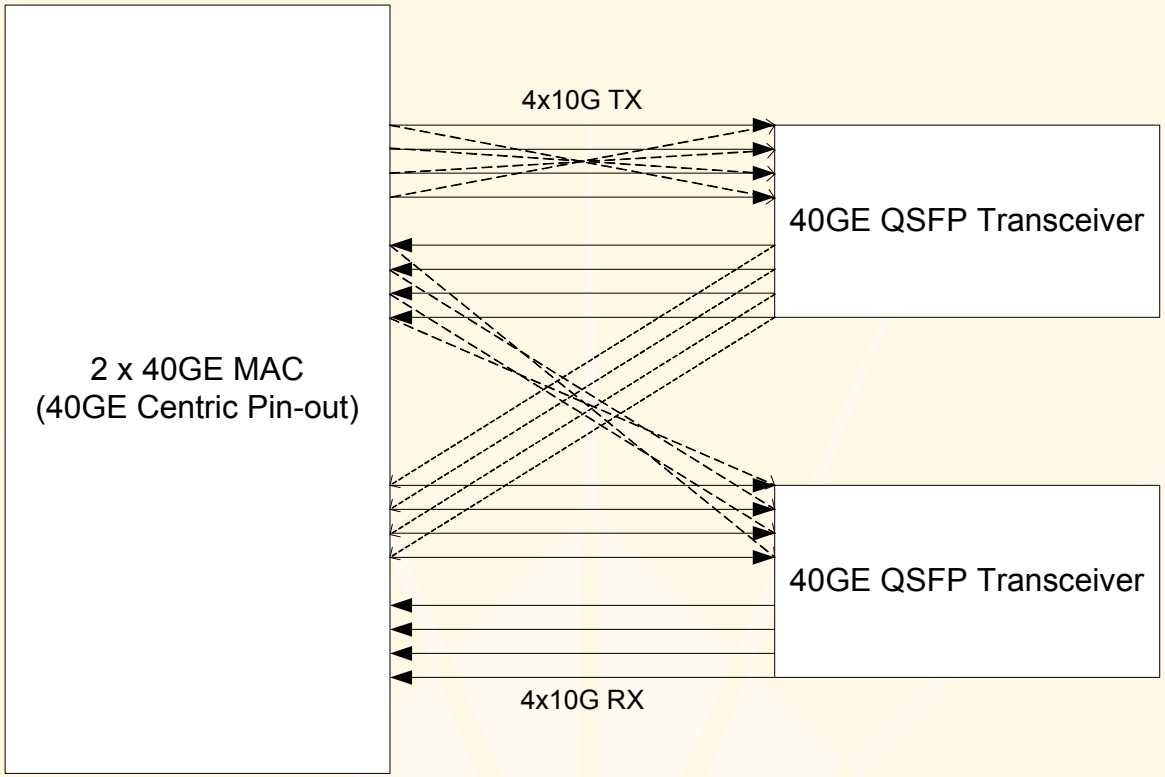
- Solid lines show interface for 100GE Centric 10G lane ordering

10G Lane Ordering: 2x40GE Mode



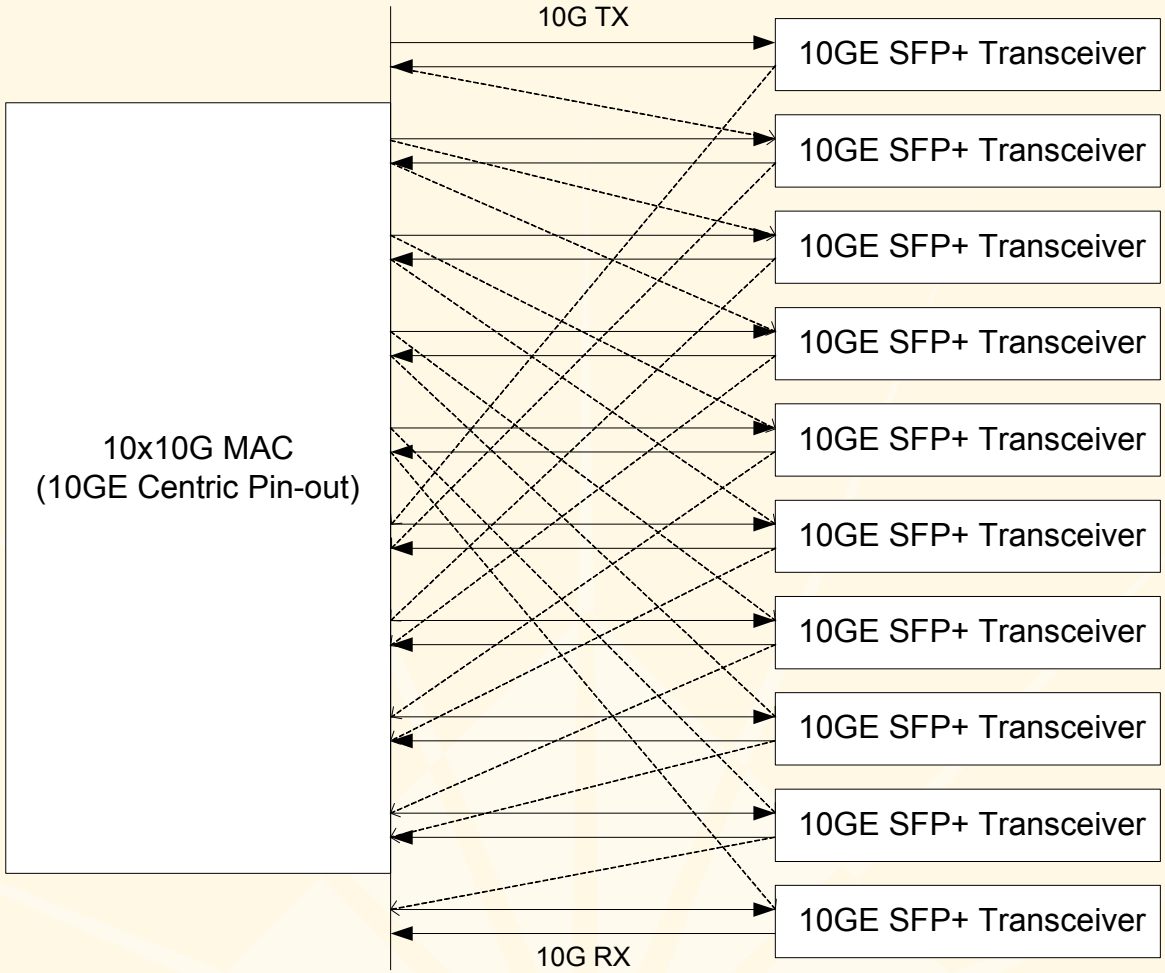
- Solid lines show interface for 40GE Centric 10G lane ordering
- Dashed lines show interface for 100GE Centric 10G lane ordering

10G Lane Ordering: 2x40GE Mode



- Solid lines show interface for 40GE QSFP Centric 10G lane ordering
- Dashed lines show interface for 100GE Centric 10G lane ordering

10G Lane Ordering: 10x10GE Mode



- Solid lines show interface for 10GE Centric 10G lane ordering
- Dashed lines show interface for 100GE Centric 10G lane ordering

10G Lane Ordering Discussion

- 10G lane ordering is important for:
  - MAC multi-mode functionality definition
  - PMD definition
  - PHY IC definition
- 10G lane ordering options
  - 100GE centric
  - 40GE centric
  - 10x10GE centric
- Interconnect alternatives between MAC and different PHYs
  - Host PCB lane re-ordering
  - PHY PCB lane re-ordering
  - Multiple MAC lane sets; each set order optimized for different PHY
  - External interface IC(s) for lane re-ordering and to buffer MAC 10G I/O from stringent electrical requirements of some PHYs like SFI Limiting for SR and LR SFP+ and SFI Linear for LRM SFP+
- Recommend 100GE centric 10G lane ordering since lane re-ordering inside 100GE PHY is most challenging

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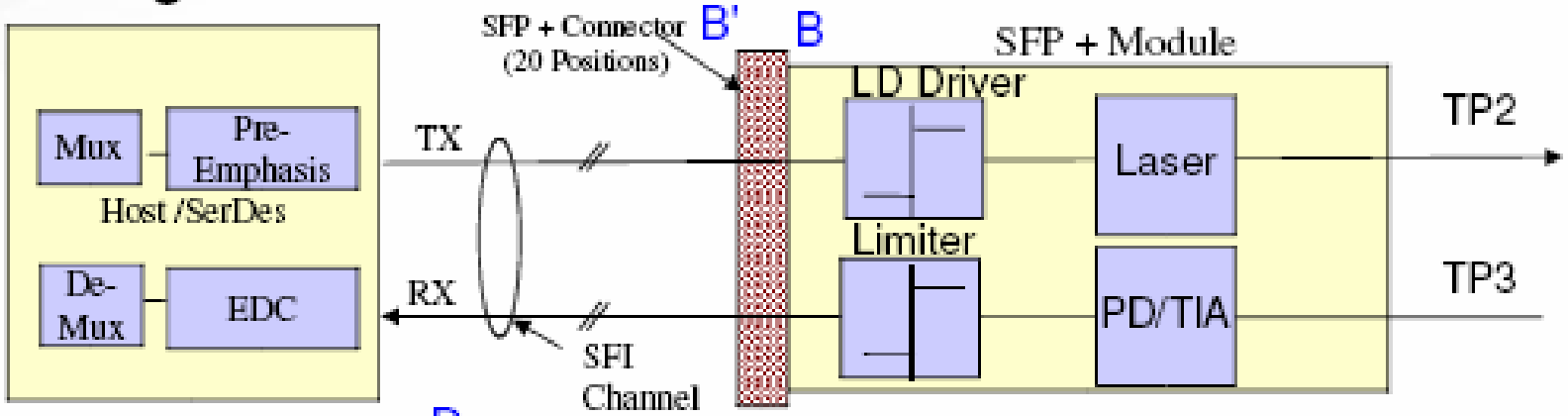
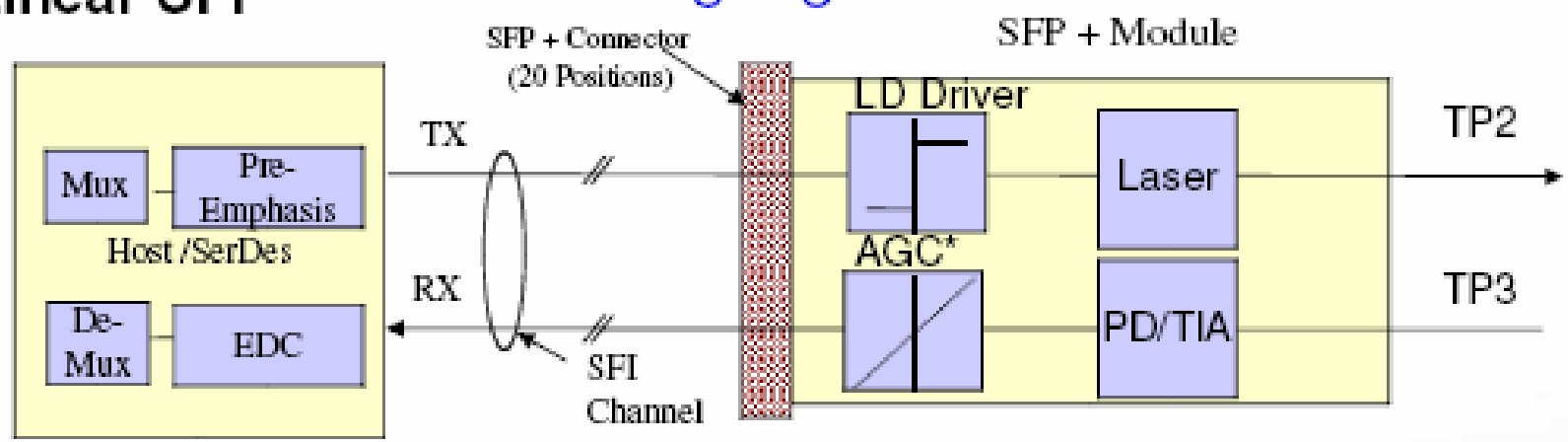
10G Jitter Budget Single Channel Model (SFP+)

- Limiting SFI



- Linear SFI



ghiasi_01_0707

10G Jitter Budget Comparison

Total Jitter (TJ) and Deterministic Jitter (DJ) values in U.I.	10x10G Jitter Budget aronson_01_0907 with updates		10x10G Jitter Budget ghiasi_01_0707 with updates	
	TJ	DJ	TJ	DJ
TP1 (B) *PMD Input from Host*	.32	.15	.36	.18
TP2 *PMD TX Optical Output*	.46	.26	.55	.33
TP4 (C*) *PMD Output to Host*	.62 meets spec	.35	.77 out of spec	.48
Proposed TP4 (C*) *TJ Specification Limit*	.62		.60	
TP4-TP1	.30	.20 ΔDJ	.39	.30 ΔDJ

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10G Jitter Budget Discussion

- Ghiasi Jitter Budget assumes severe host cross-talk effects and higher TP4-TP1 ΔDJ then Aronson Jitter Budget resulting in higher TP4 TJ which exceeds proposed spec
- The higher TP4 TJ includes more margin than required by 10GE spreadsheet model for a 100m OM3 link with reasonable assumptions on transmitter and receiver performance
- To resolve these differences:
  - Cross-talk effects will have to be quantified using measurement results from multiple contributors
  - "I would encourage all IC vendors participating in the HSSG, who have developed silicon that implements 10G I/O, to bring in multi-lane 10G I/O cross-talk data so that we can base the 40G and 100G specifications on measurement results." (6/28/07 Cole email to 802.3 HSSG reflector)
  - Assumptions about transmitter and receiver parameters for use in 10GE spreadsheet model will need agreement

10G Jitter Budget and RX Equalizer Considerations

- RX EQ can only reduce DDJ (Data Deterministic Jitter) part of TJ
- RX EQ can not reduce cross-talk effects
- RX EQ with Linear TIA can reduce DDJ between TP1 and TP4

  (RX EQ with Limiting TIA can not reduce DDJ between TP1 and TP4)
- If host or other cross-talk effects are found to be more severe, then a RX Echo Canceller will be required to meet the TJ spec. In that case, there will be not be enough DDJ between TP1 and TP4 for RX EQ to remove to offset the cross-talk effects.
- Conclusions from requested cross-talk effects measurements:
  - If crosstalk is “moderate”, RX EQ + Limiting Interface is OK
  - If crosstalk is ‘severe”, RX EQ + Linear Interface is required
  - If crosstalk is “more severe”, RX Echo Canceller is required
- Last two outcomes may require separate SMF and MMF 10G I/O specs to not burden SMF applications

Lane Encoding Discussion

- Two proposals for 40GE and 100GE Nx10G lane encoding
  - Virtual Lane (VL) ex. “CTBI” for 100GE
  - APL
- Implications for 40GE PHYs
  - 4x10G Electrical I/O Interface
  - 4x10G or 1x40G Optical Interfaces
  - Simple implementation and testing for VL and APL
  - No preference for VL or APL (same PHY IC implementation)
- Implications for 100GE PHYs
  - 10x10G Electrical I/O Interface
  - 4x25G Optical Interface
  - Simple implementation and testing for VL. PHY IC is 10:4 bit Mux and DeMux with small FIFOs to absorb wander
  - Complex implementation and testing for APL. PHY IC is fragment Mux and DeMux with header processing and large FIFOs
  - Recommend VL to avoid PHY IC complexity, size and development problems, similar to ones caused by XAUI for 10GE PHYs
- Conclusion: Put the PCS in the MAC (cole_02_0307, p.5)

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Summary

- 100GE centric 10G lane ordering is recommended
- Nx10G Electrical I/O cross-talk data is requested from multiple contributors to enable jitter quantification and link budget development
- Virtual Lane encoding is recommend to minimize 100GE PHY complexity and development problems