Comparisons of Linear vs Limiting Electrical Interface for 4x10G and 10x10G

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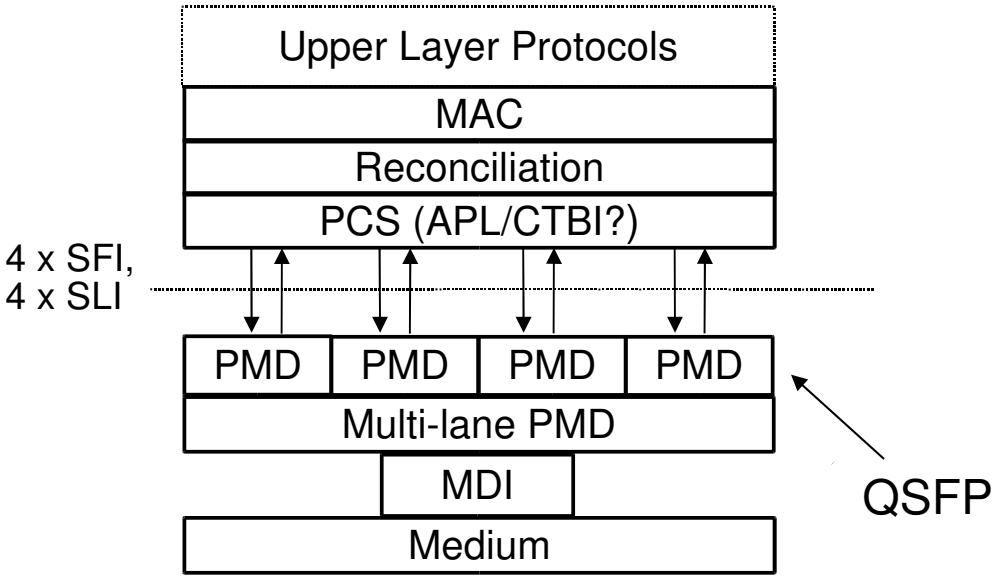
Overview

- The current assumption is not to use CDR in the 4x and 10x modules due to power dissipation and added cost.
- SFI single lane limiting specifications will be too difficult for 4x and 10x links.
- TX pre-emphasis and EDC either adaptive or non-adaptive will be used for all implementations to overcome FR4 losses.
- Limiting module specifications would be difficult to close even if the fibre reach is reduced from 300 m to 100 m on OM3 due to transmit DDJ.
- Linear module specifications with adaptive EDC provides extra margin to close the link without using CDR in the module.
- Propose SLI as the electrical interface which is light version of SFI.

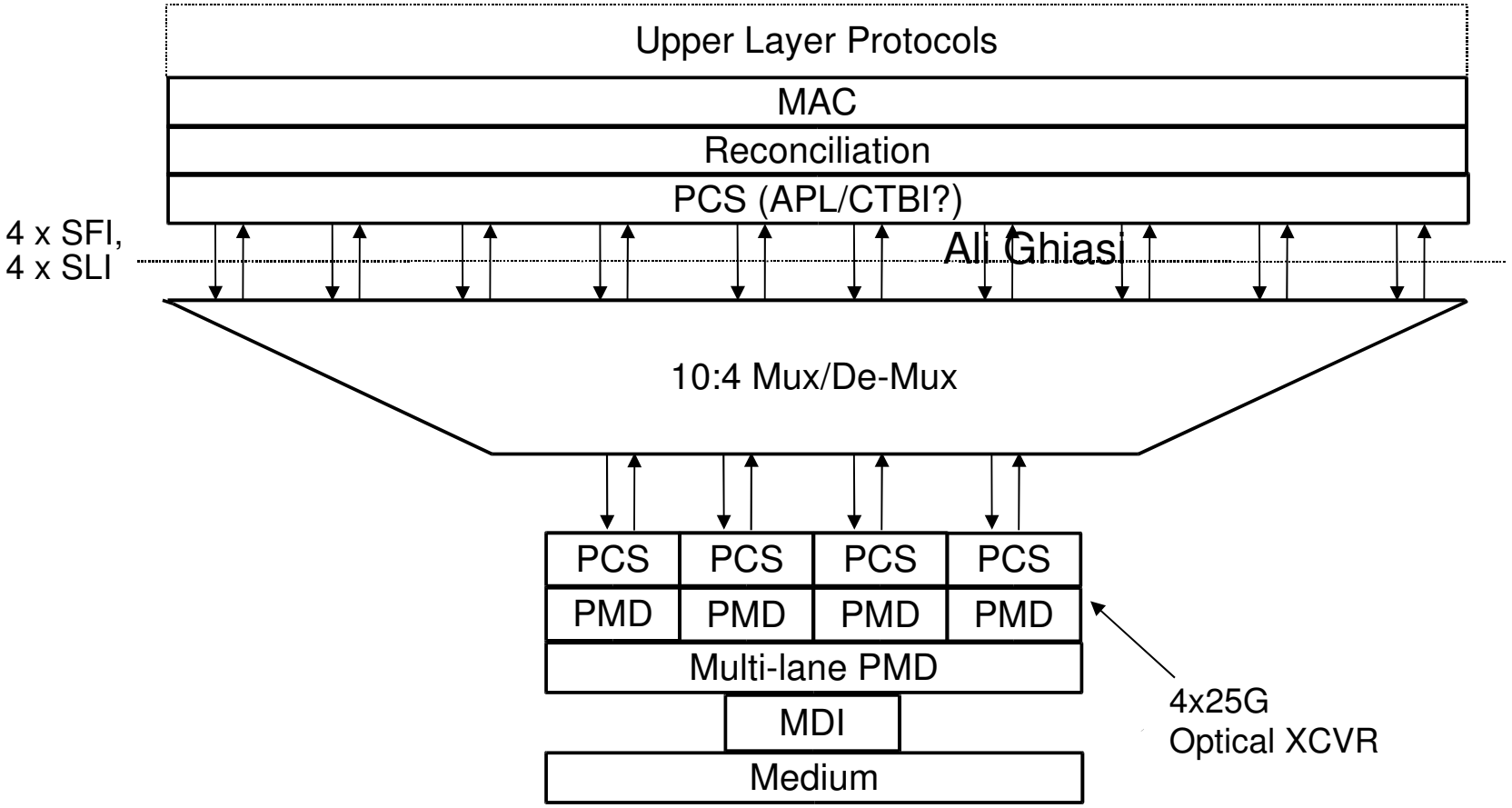
PMA interface for the 4x10G

- **SFI chips early on can enable the market.**



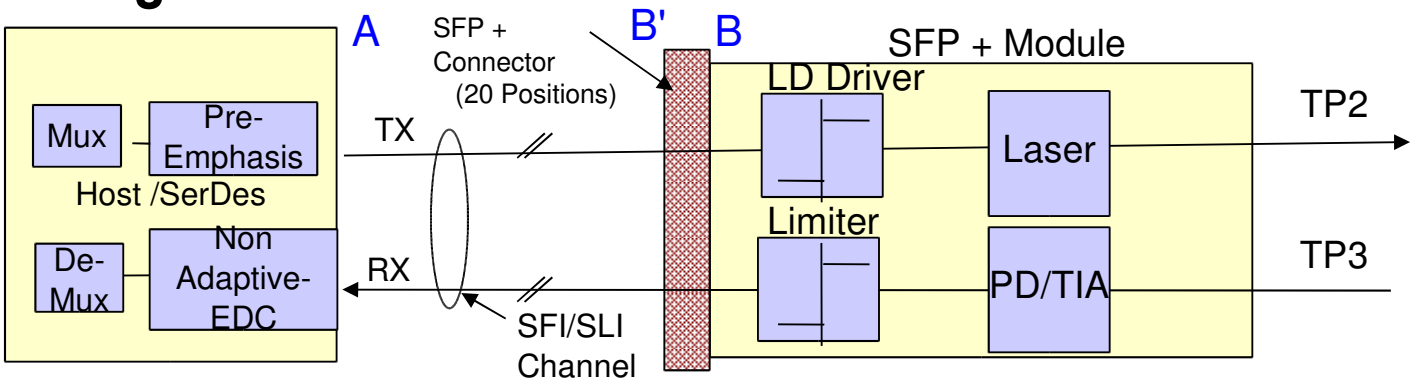
PMA interface for the 4x25G

- **Same interface can support 10x10G**

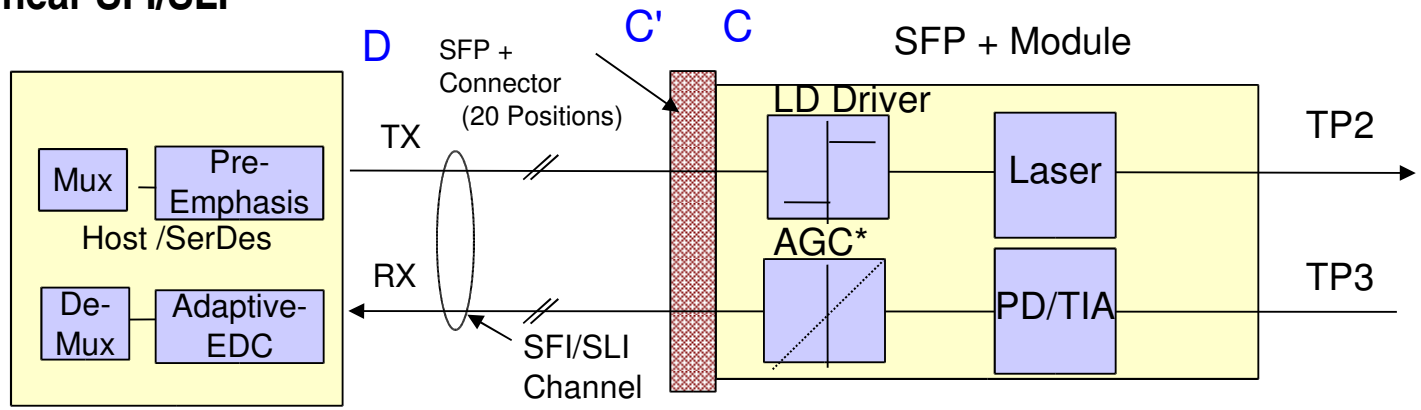


Block Diagram Limiting and Linear SFI/SLI

- **Limiting SFI/SLI**



- **Linear SFI/SLI**



* Common implementation incorporates AGC in the PD/TIA

The Benefit of Linear Module Interface with Adaptive EDC

- EDC allow using slower lasers and detectors
- Allow longer fibre reach
- Support longer FR4 PCB traces
- No need for the CDR in the module
  - Enable smaller form factor
  - Lower power dissipation
- Lower cost
- Potentially common host chips with the backplane and copper cable.

4X/10X Jitter Degradation Starting with SFI

- **SFI DDJ at B=0.1 UI**
  - **DDJ at Host Output (B) for 4x link is expect at least 0.15 UI**
  - **DDJ at Host Output (B) for 10x link is expected to be at least 0.18**

Degradation	4x Jitter (UI)	10x (UI)
SFI B	0.100	0.100
SerDes Penalty	0.025	0.040
PCB Routing	0.025	0.040
Total DDJ B	0.150	0.180
Total TJ B	0.320	0.360

Degradation	4x Jitter (UI)	10x (UI)
SFI C'	0.7	0.7
SerDes Penalty	-0.04	-0.07
PCB Routing	-0.02	-0.03
TJ at C'	0.64	0.6

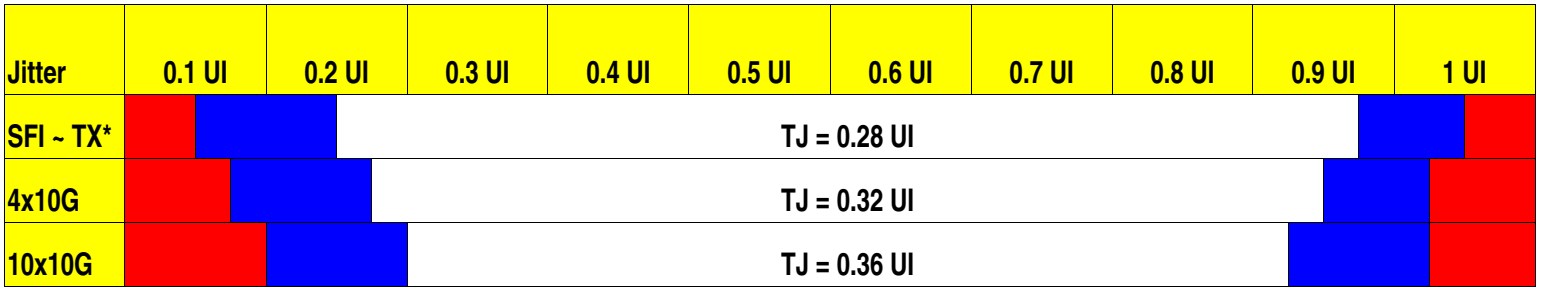
Starting Limiting Jitter Budget

- **Assumption made**
  - **10x10 Gig optics is given no excess penalty**
  - **DJ would increase by 0.05 UI**

Jitter Compliance Points	B	TP2	Fiber	TP3	C*
4x10Gig					
DJ UI	0.150	0.300	0.050	0.350	0.450
TJ UI	0.320	0.500		0.550	0.715
1-sigma RJ at max DJ for BER 1E-12 (ps)	1.178	1.386		1.386	1.836
10x10 Gig					
DJ UI	0.180	0.330	0.050	0.380	0.480
TJ UI	0.360	0.550		0.600	0.765
1-sigma RJ at max DJ for BER 1E-12 (ps)	1.247	1.524		1.524	1.975

Eye Opening at Host TX Output (B)

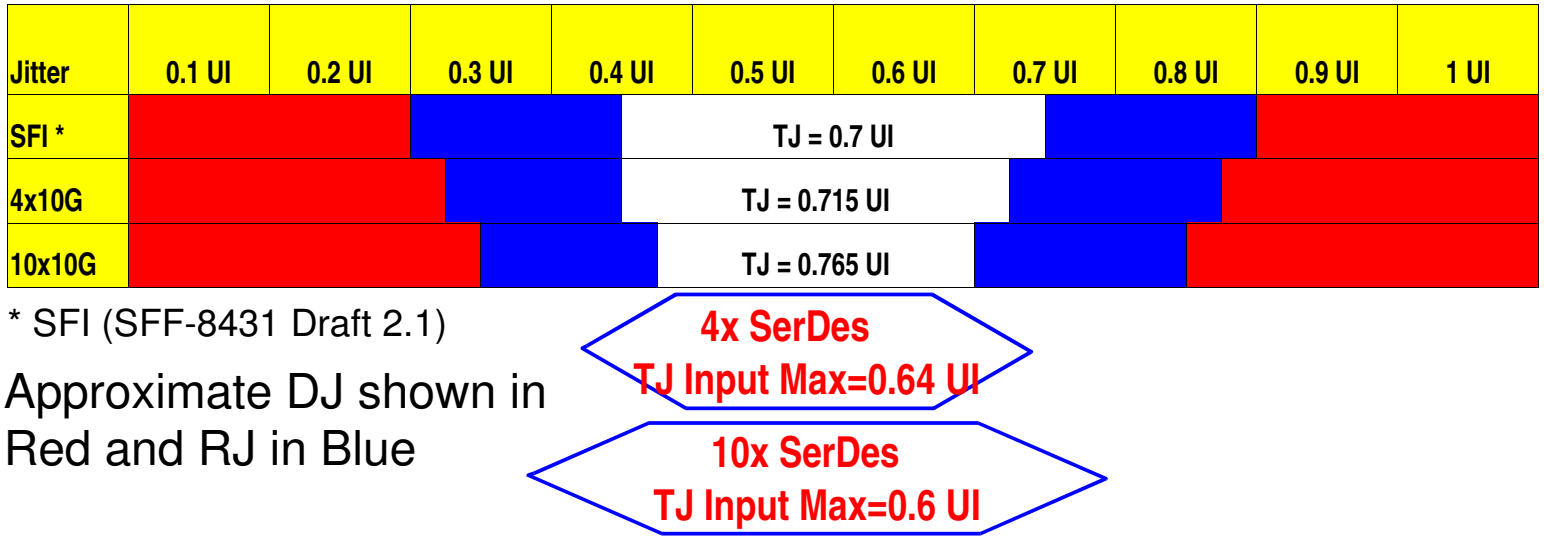
- **4x10G host output is expected to be slightly worse than SFI and the jitter value are similar to 8 GFC.**
- **10x10 G is about 0.05 UI worse than 4x10G**



Approximate DJ shown in Red and RJ in Blue

* SFI (SFF-8431 Draft 2.1)

Eye Opening at Host RX Input (C)



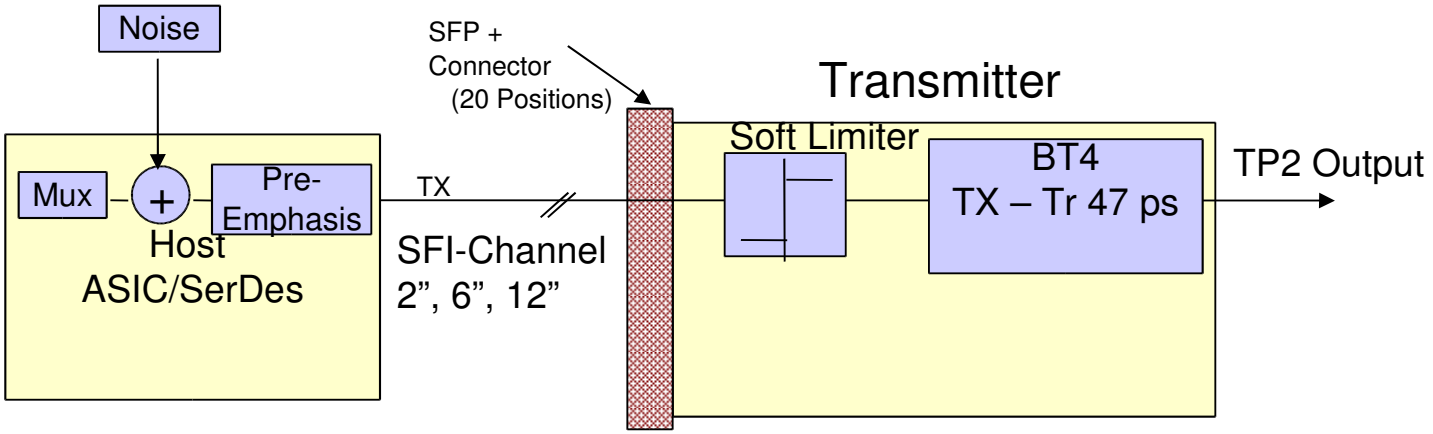
- **4x and 10x Jitter budget can not be closed reliably for limiting interface**

  When the module output TJ exceed the SerDes maximum input jitter the link does not close:

  - **The option is to use a linear receiver with lower overall cost and power**

SFI TP2 Simulation Set-up

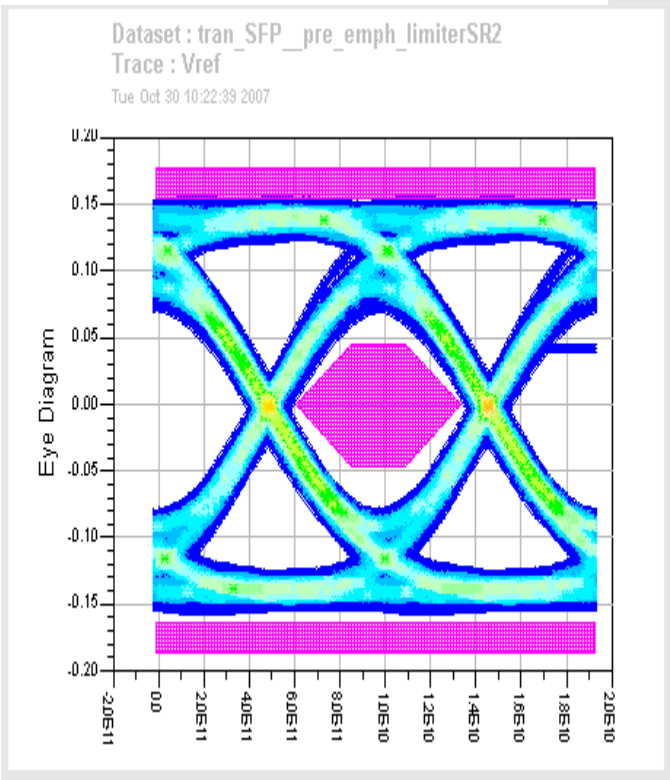
- **RIN penalty is not included**
- **2 inch stripline channel was inserted**
- **Noise source at the SerDes was adjusted for UJ of ~0.023 UI (RMS) at B.**
- **BT4 filter in the module was adjusted for Trise/fall of 47 ps 20-80%.**
- **Results shown is for optimum pre-emphasis**



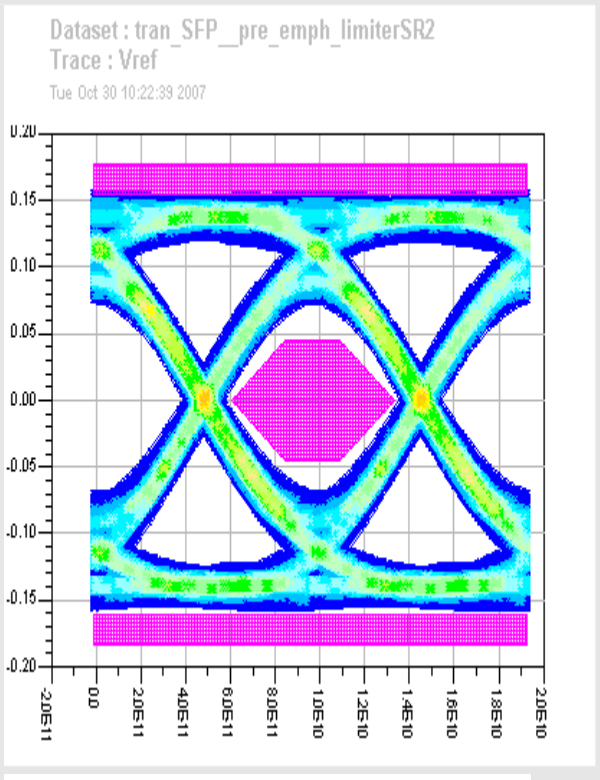
SFI Transmitter Output with Optimum Pre-emphasis

- **Pre-emphasis single T-Spaced post**
  - **Eye mask will get degraded further due to PCB and IC variations!**

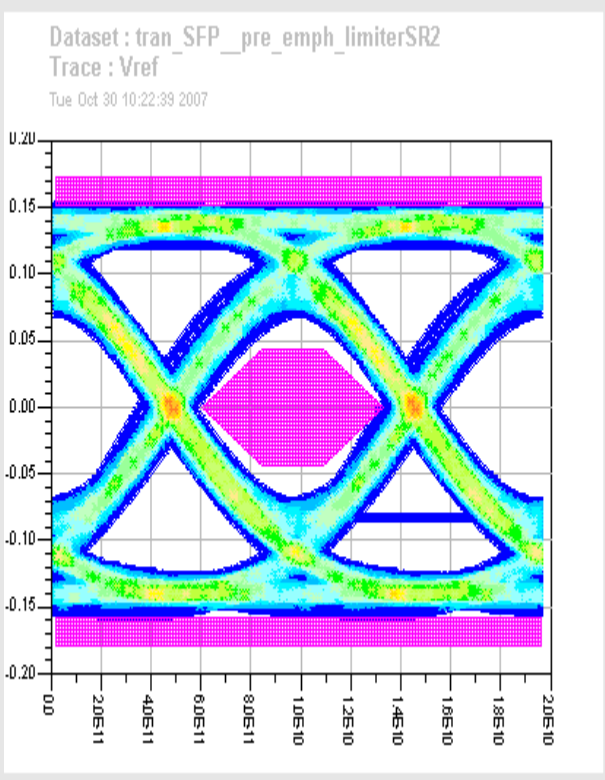
2” Fr4-13



6” Fr4-13



12” Fr4-13



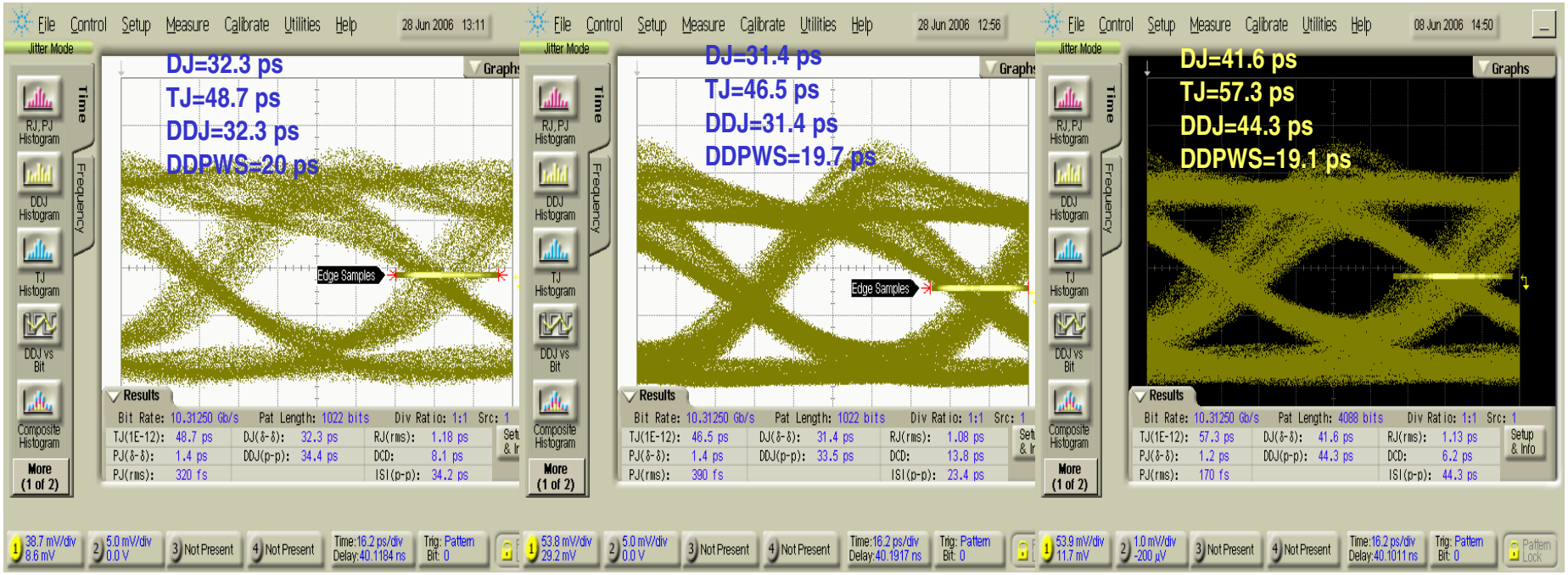
Eye Diagram for 3 Sub-10G Transmitters

- **aronson_01_0907.pdf stated parallel link need more margin so we started with 3 sub-10G transmitters**
  - **The lasers DJ and TJ are similar to the jitter spreadsheet on page 9 at TP2!**

Supplier-A

Supplier-B

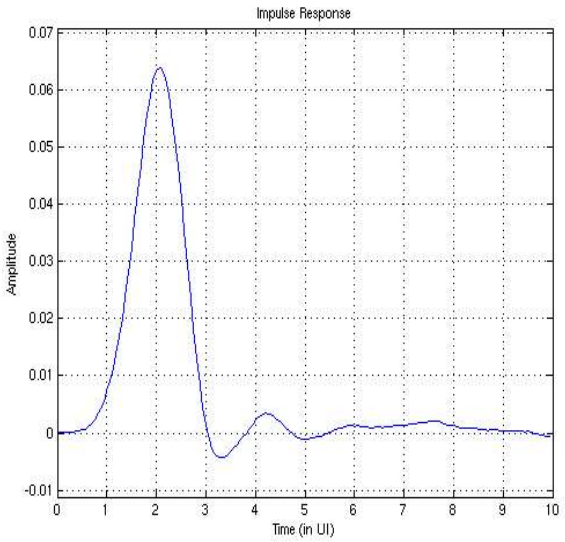
Supplier-C



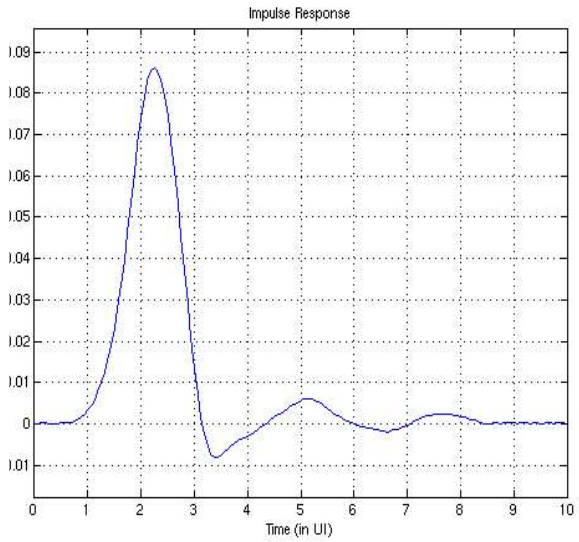
Impulse for 3 Sub-10G Transmitters

- **All 3 lasers exhibit strong pre-cursor**

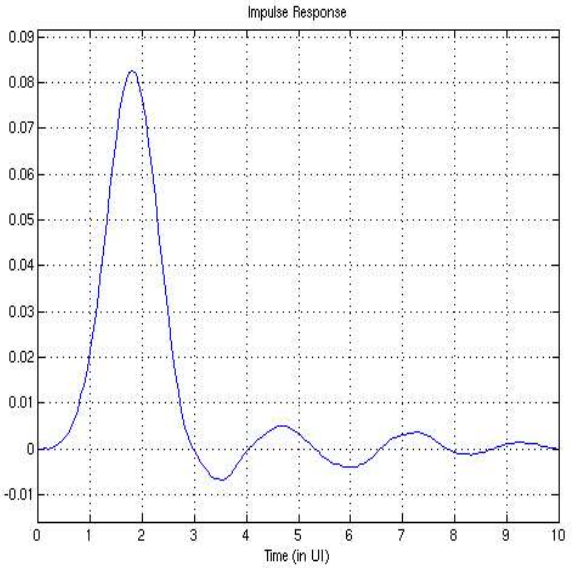
Supplier-A



Supplier-B

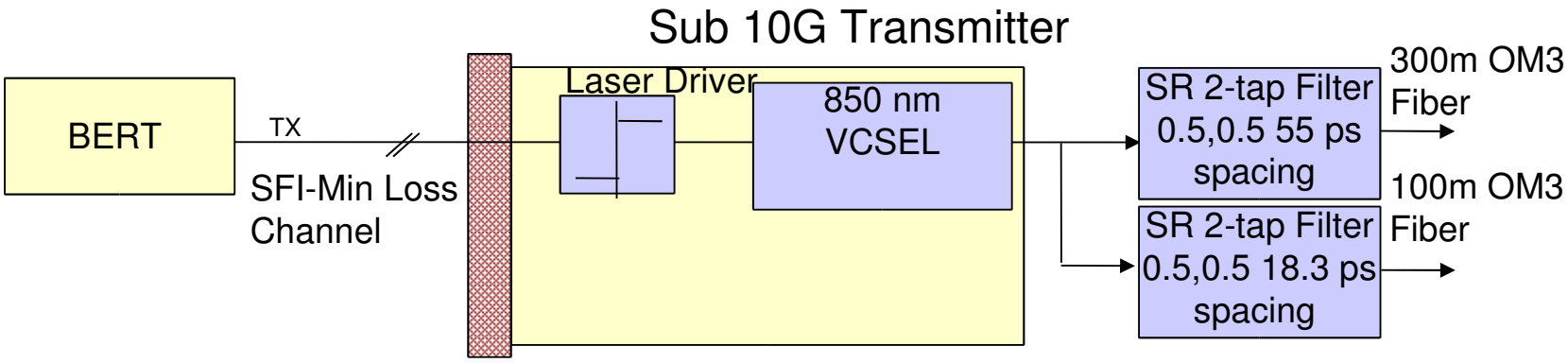


Supplier-C



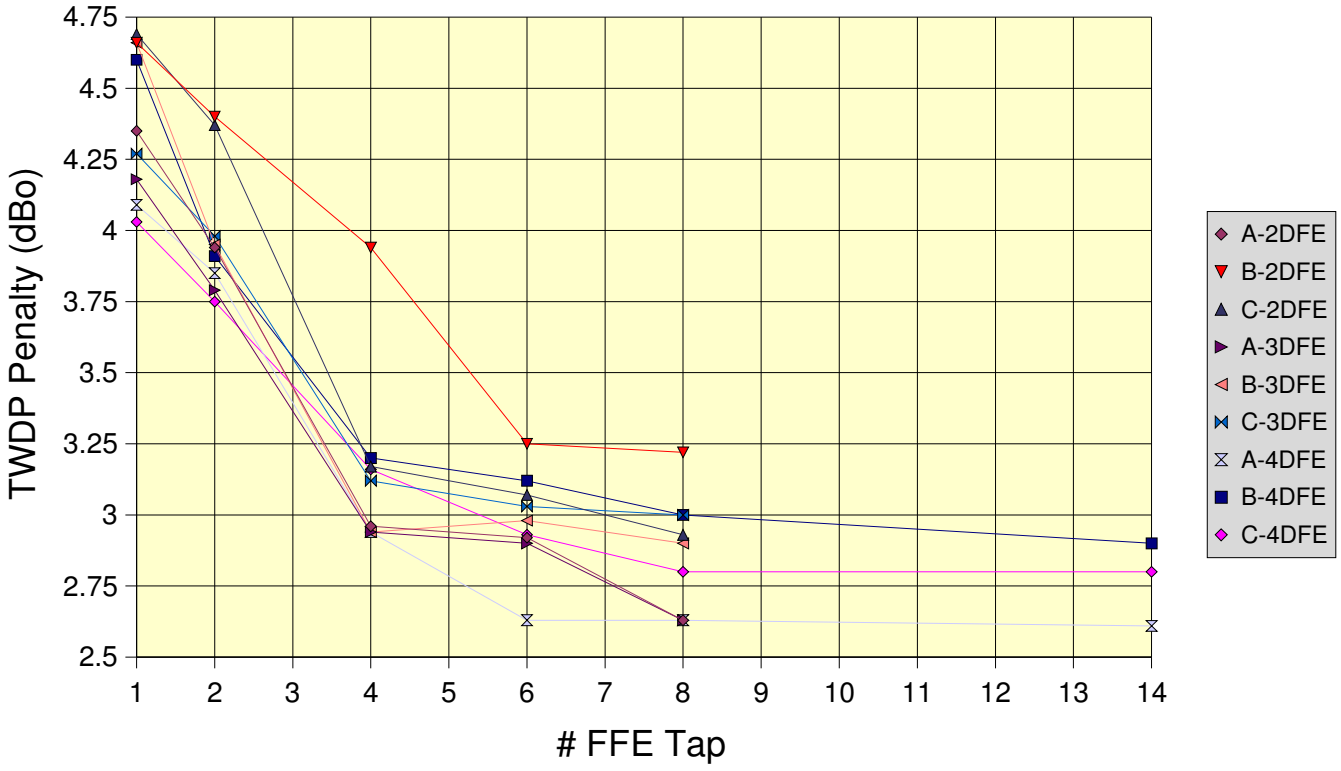
TWDP Simulation Set-up

- **Code based on IEEE 802.3 CL 68**
- **LRM stressor in the IEEE code were replaced with**
  - **2-tap FIR filter (0.5,0.5) with 55 ps delays to emulate 300 m OM3 fiber as defined by IEEE 802.3 CL 52**
  - **2-tap FIR filter (0.5,0.5) with 18.3 ps delays to emulate 100 m OM3 fiber**



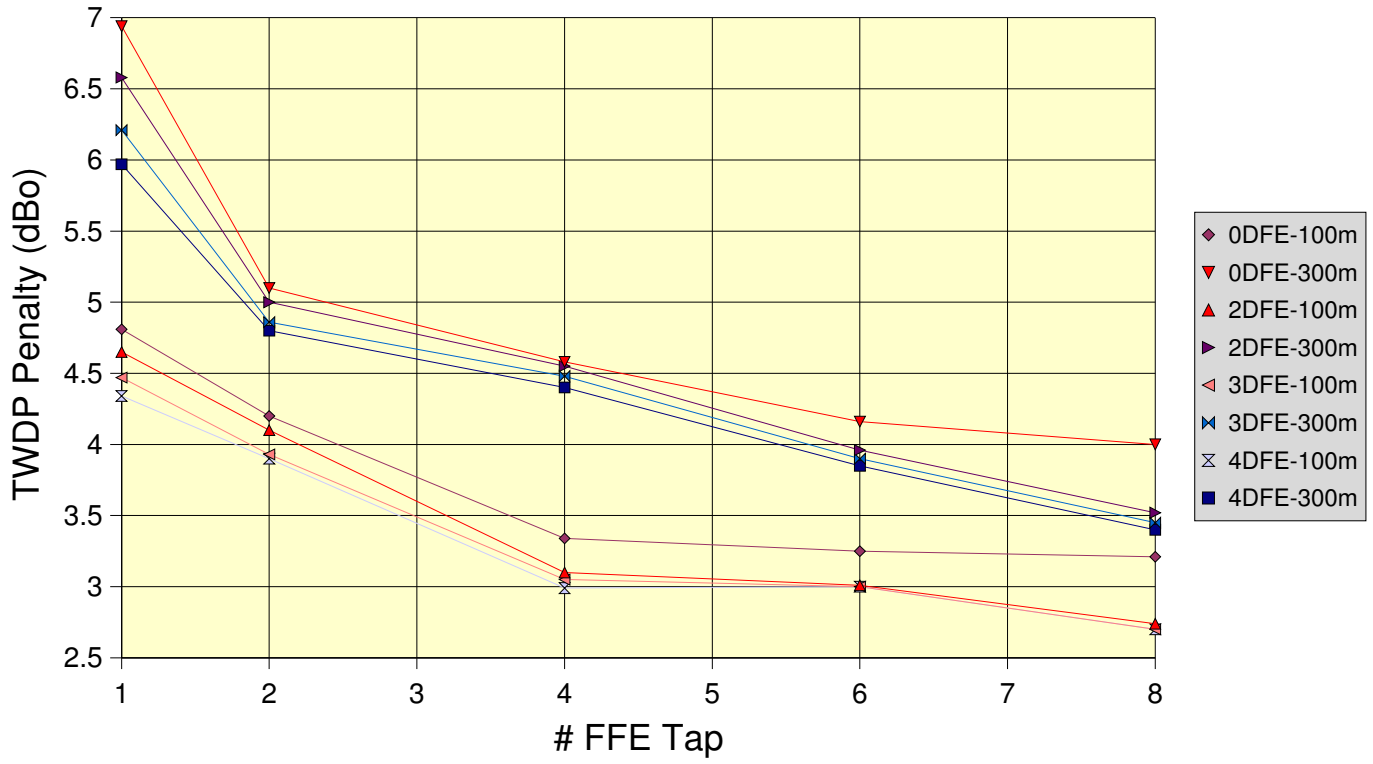
TWDP Penalty as Function of FFE and DFE Taps (no fibre stressor)

- **Based on the study of 3 suppliers A, B, and C sub 10G transmitters**
  - **Fiber and the RX electrical PCB/connector not included**
  - **Min reference receiver would be 4 T/2 FFE+2 T DFE**



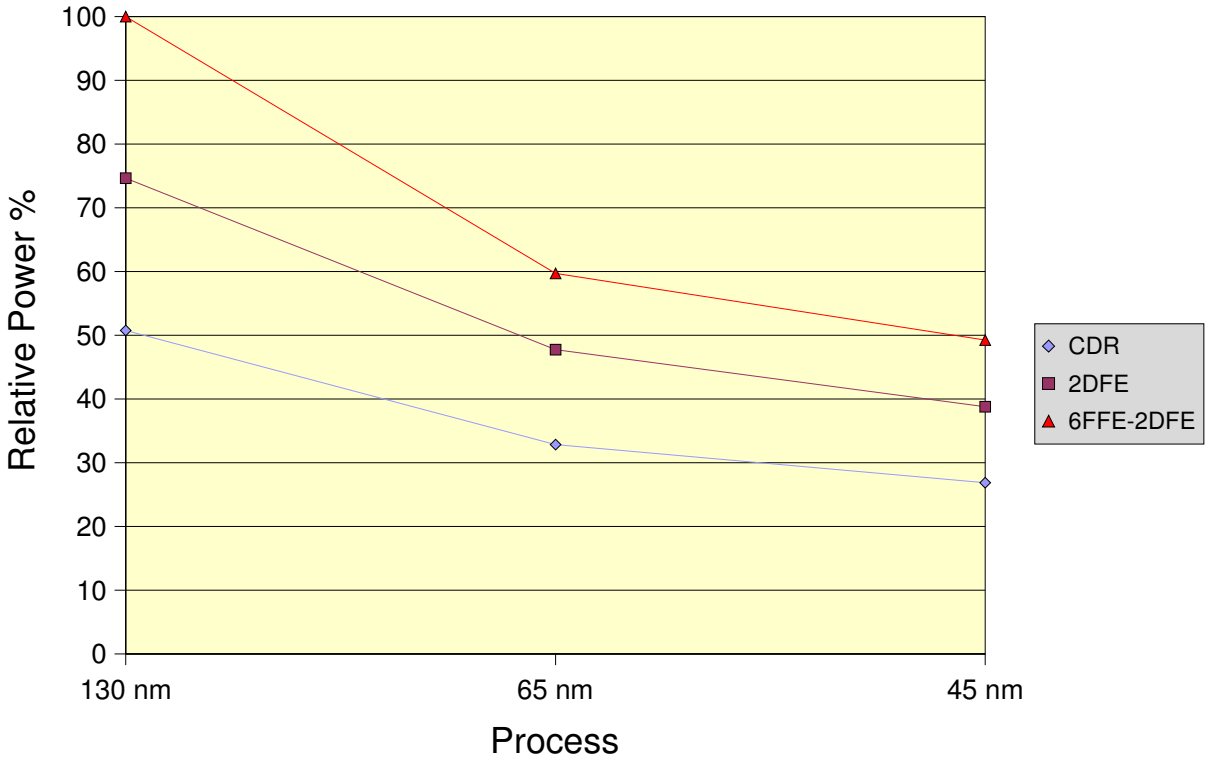
WDP Penalty as Function of FFE and DFE Taps for 100m and 300

- **Transmitter A response with 100m and 300 m of OM3 fiber**
  - **RX electrical PCB/connector not included**
  - **Reference receiver with 4 T/2 FFE+2 T DFE should be sufficient for 100m**
  - **Reference Receiver with 6 T/2 FFE+ 2 T DFE should be sufficient for 300m**



Relative Power of the Host Receivers

- **The limiting interface due to FR4 traces and connector require ~2 tap DFE+CDR.**
- **The linear interface require 4 to 6 tap T/2 FFE + 2 to 3 tap DFE+CDR.**
- **Increasing the limiting receiver EQ taps to support linear has overall cost and power advantage over putting a 2nd CDR in the module!**



Compatibility Requirement Between Limiting and Linear Interfaces

- **Propose use of linear and limiting module**
  - **All modules with a mux will be limiting**
  - **All modules with 10G baudrate and without a mux will be linear.**
  - **A limiting module can plug in to a linear host**

Solution	Link Bit Rate (Gb/s)	Elec Lanes	Elec Symbol Rate (Gbaud)	Limiting Module	Linear Module	Retime Module	Compatible with Adp EDC Host
XFP	10	1	10	x		x	x
SFP+ (Limiting)	10	1	10	x			x
SFP+ (Linear)	10	1	10		x		x
4x10G (SR)	40	4	10		x		x
10x10G (SR)	100	10	10		x		x
4x25G Gen 1	100	10	10	x		x	x
4x25G Gen 2	100	4	25	x		x	TBD

Conclusion

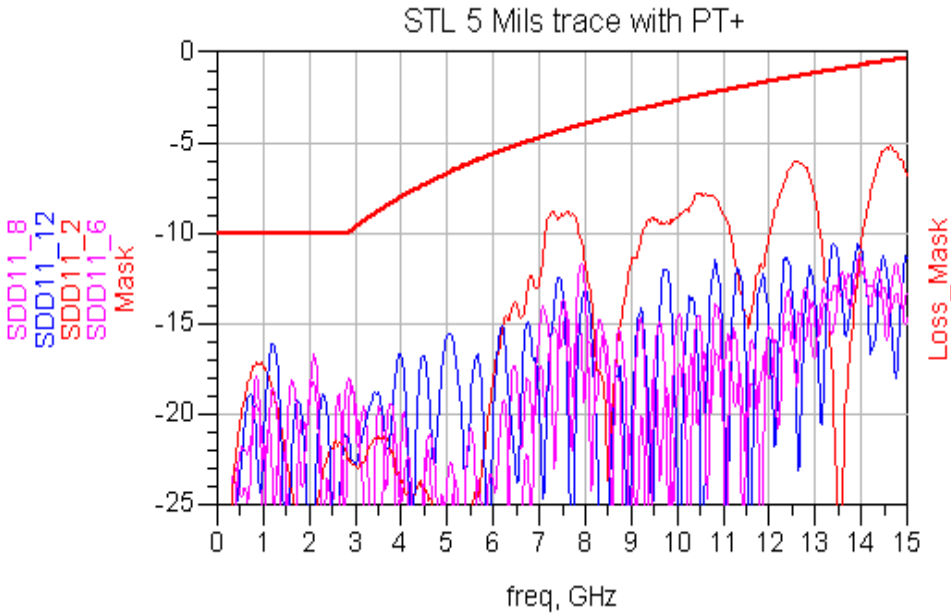
- SFI limiting jitter specifications are very challenging and would be very difficult to scale to 4x and 10x limiting link.
- Use of linear interface with adaptive EDC can allow
  - Relaxing SerDes transmitter
  - Relaxing SerDes receiver
  - Allowing more margin for the host implementations
  - Common electrical interface for 4x and 10x
  - Use lower cost optics.
  - Possible SerDes chip commonality with copper cable and backplane.
- Linear can do 300 m with about 1 dB less penalty than limiting can do 100 m!

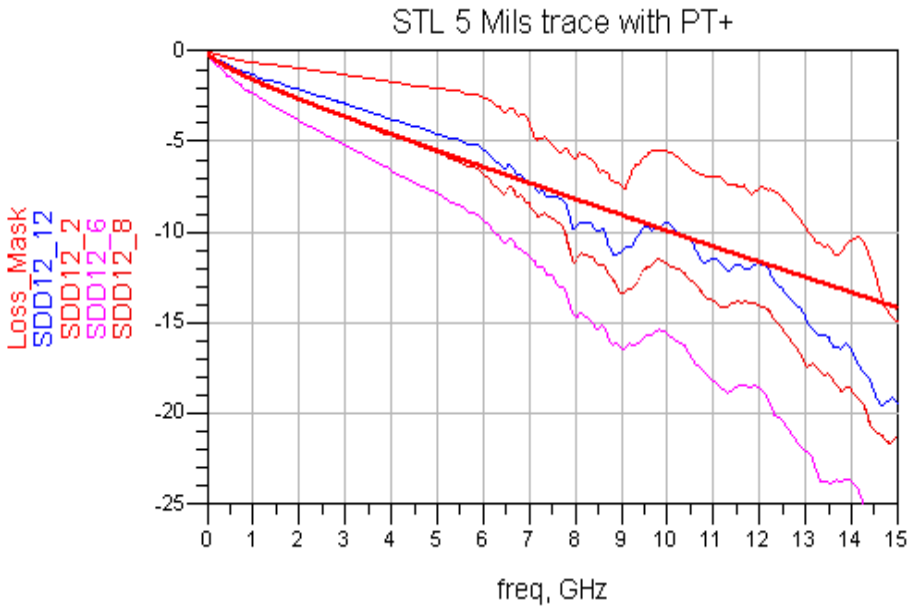
Reference Material/Back Up Material

- For detail description of linear and limiting interface see: “Next-generation 10 GBaud module based on emerging SFP+ with host-based EDC”, IEEE Communications Magazine, vol. 45, no. 3, March2007, pp. 32 - 38
- DDJ – Data Dependent Jitter
- DDWPS – Data Dependent Pulse Width Shrinkage
- TDP – Transmitter Dispersion Penalty see IEEE 802.3 CL 52
- TWDP – Transmitter Waveform Dispersion Penalty see IEEE 802.3 CL68
- WDP – Waveform Dispersion Penalty see SFF-8431 ftp://ftp.seagate.com/sff/SFF-8431.PDF

SFI Reference Channels

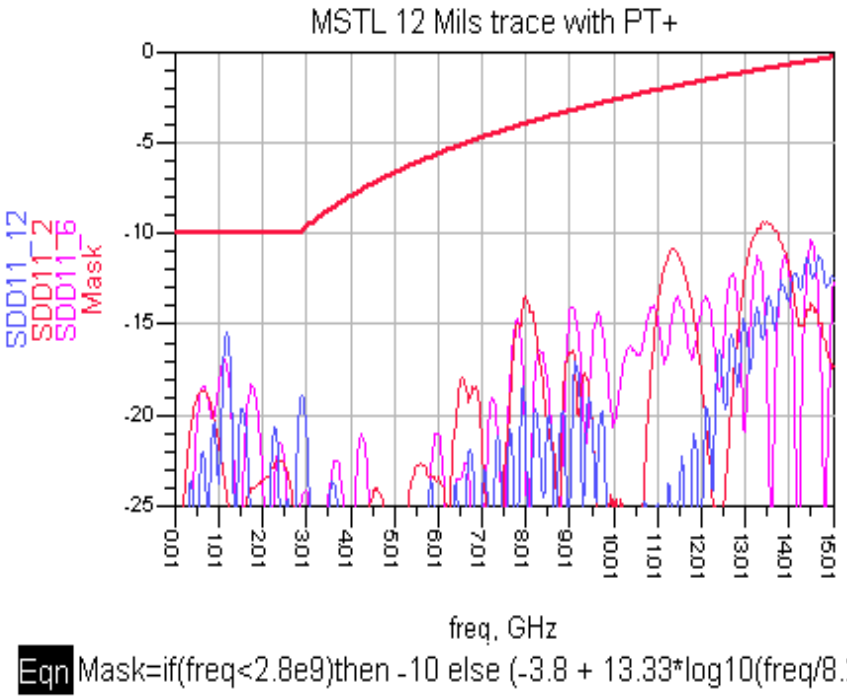
- **5 mils Stripline channels with 2”, 6”, 8”, and 12” length**
  - **Traces include 2 via stubs**
  - **Include the PT enhanced connector (XFP, SFP+)**
  - **s4p files provided by Broadcom are available for the striplines and a set of microstrip channels from www.t11.org doc # T11 06-683v0**

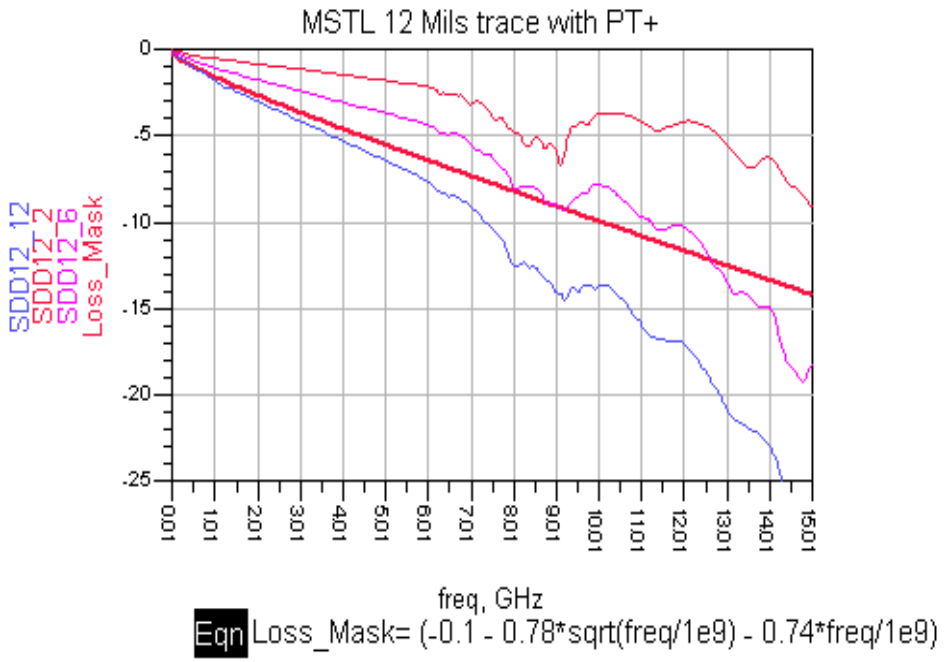




SFI Reference Channels

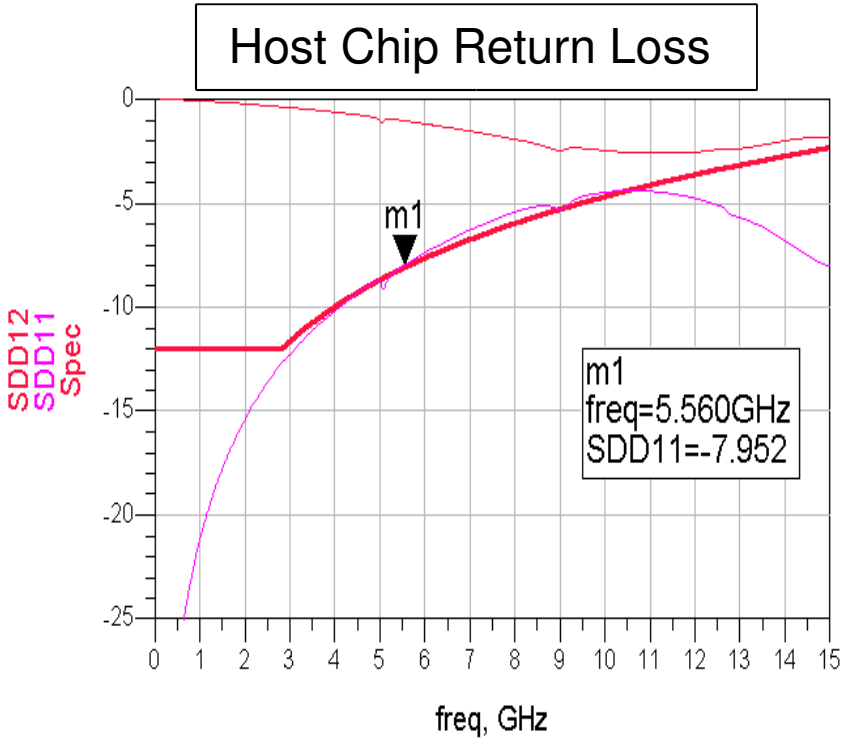
- **12 mils Microstrip channels with 2”, 6”, 8”, and 12” length**
  - **Include the PT enhanced connector (XFP, SFP+)**
  - **s4p files provided by Broadcom are available for the striplines and a set of microstrip channels from www.t11.org doc # T11 06-683v0**



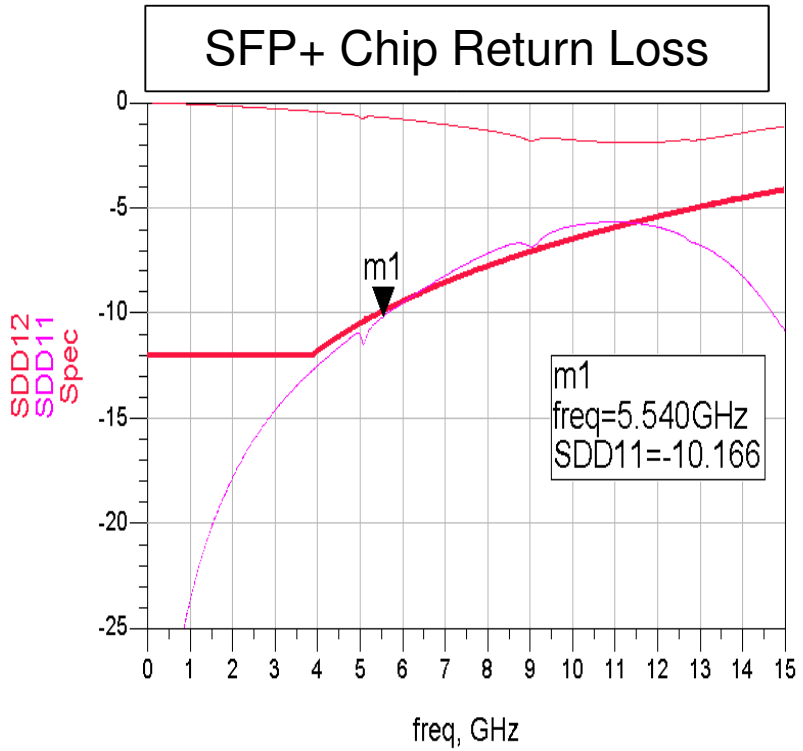


Informative Return Loss for Host and SFP+ Chips for 10-11Gig

- **More relax than XFI and similar to OIF CEI**
  - **Based on distributed models**
  - **Host chip 06-236v0 and SFP+ chip is 06-237v0 can be downloaded from T11 website.**



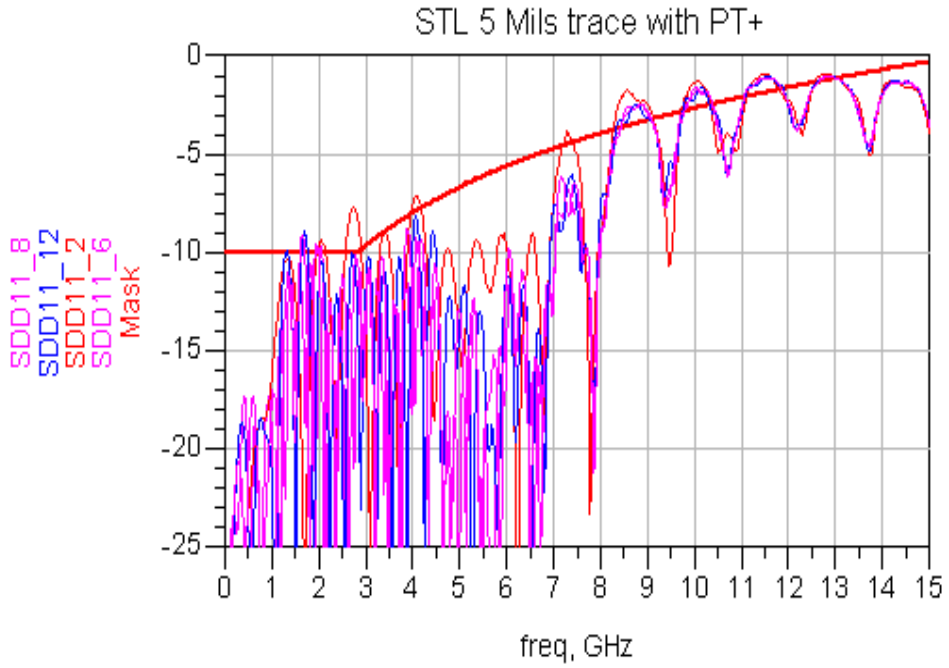
Eqn Spec=if(freq<2.8e9)then -12 else (-5.8 + 13.33*log10(freq/8.25e9

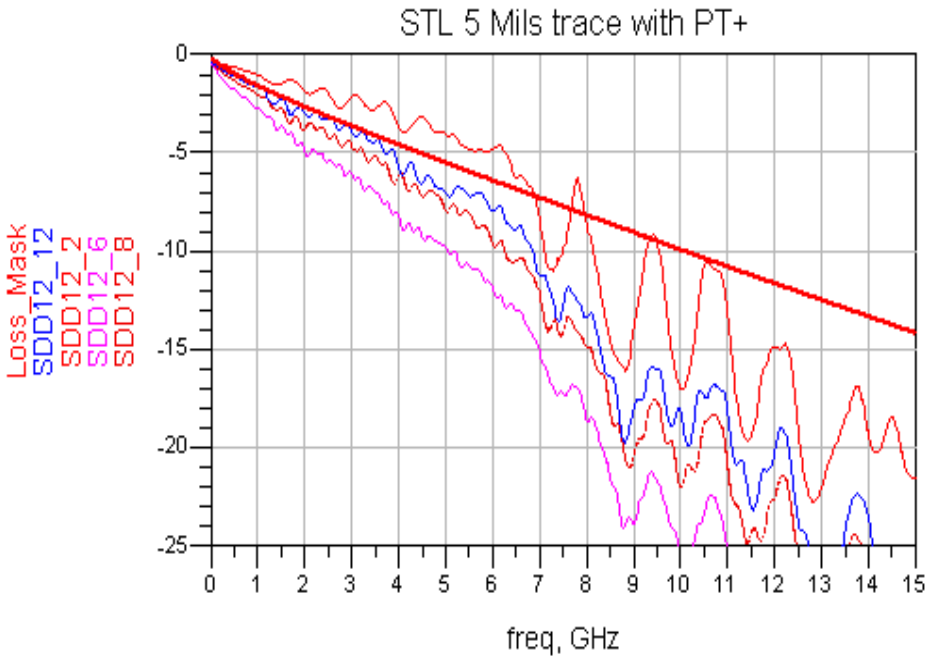


Eqn Spec=if(freq<3.9e9)then -12 else (-7.6 + 13.33*log10(freq/8.25e9))

End to End Path Stripline

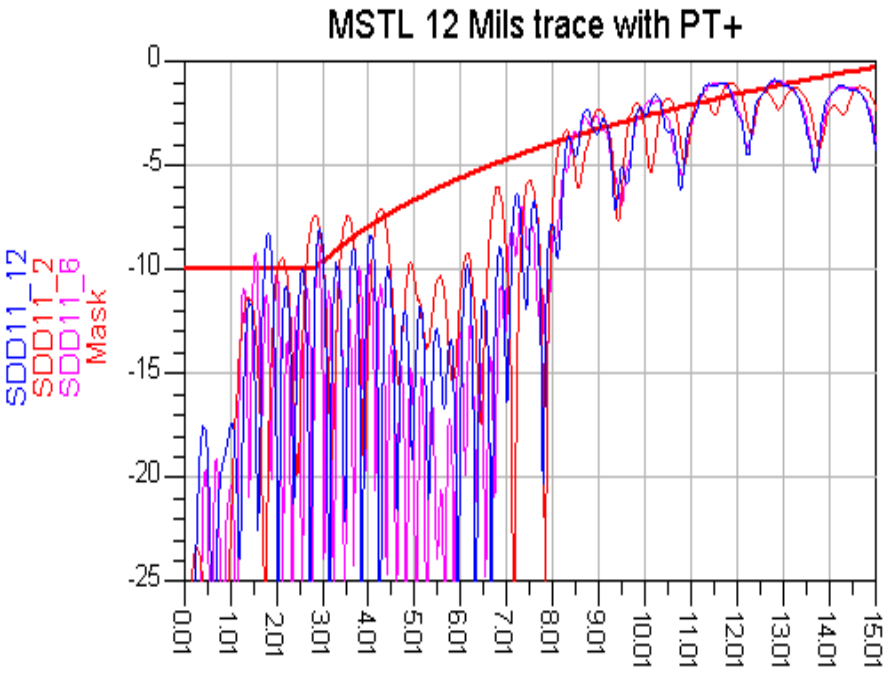
- **Channel Response cascaded with the host IC and the module IC termination model T11 06-236v0 and 06-237v0**

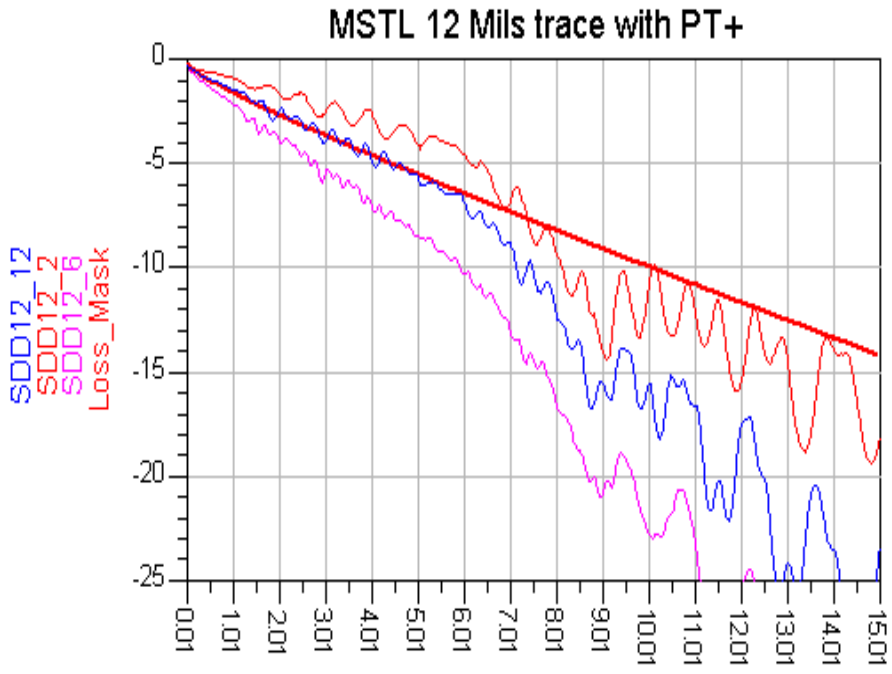




End to End Path Microstrip

- **Channel Response cascaded with the host IC and the module IC termination model T11 06-236v0 and 06-237v0**



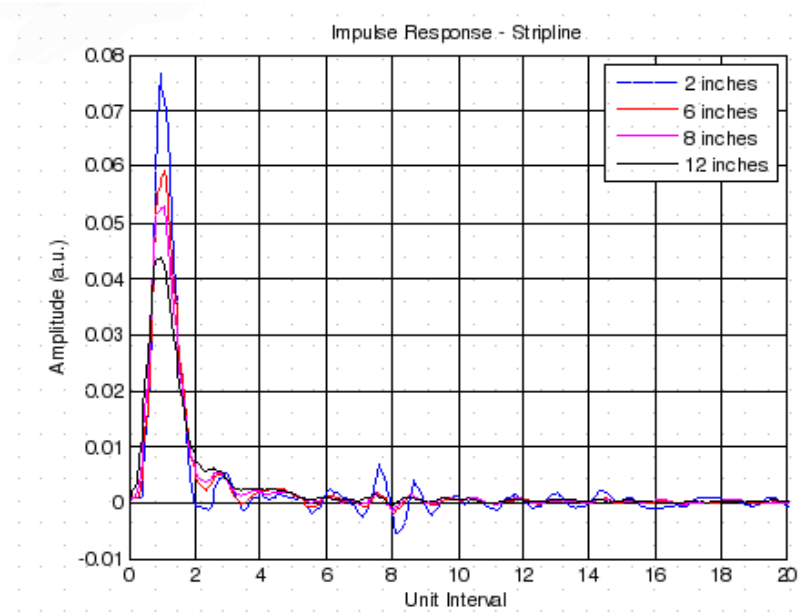


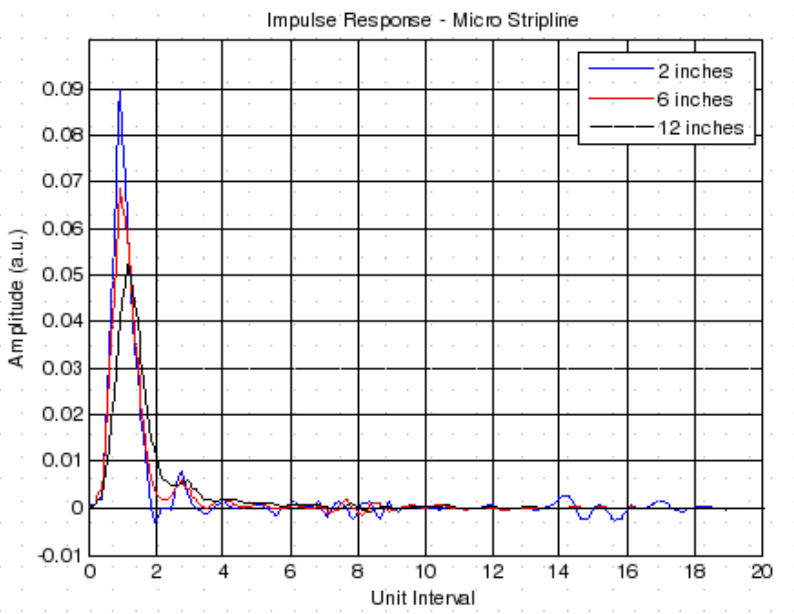
Eqn Mask=if(freq<2.8e9)then -10 else (-3.8 + 13.33*log10(freq/8.25e9)

Eqn Loss_Mask= (-0.1 - 0.78*sqrt(freq/1e9) - 0.74*freq/1e9)

Channel End to End Impulse Response

- **Each UI=97 ps**





Transmitter/Limiter Model

- **Limiter based on Hyperbolic Tangent**
  - **Soft limiter with 20 dB gain to emulate laser driver**

$$Vo = \mathrm{Vi} - \left[\left(Vsx \ tanh \left(G * Vi / Vs \right) \right) \right]$$

    - **G=10 is the limiter Gain**
    - **Vs=400 is the saturated output level**
    - **Vi from -250 to 250 mV**
- **Laser is modelled currently as 47 ps rise time**

Limiter Response

- **With loading effect the output will be from -200 to 200 mV.**