PBL Model Update

Trey Malpass
Ye Min
Ding Chiwu
Zengli

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HUAWEI TECHNOLOGIES Co., Ltd.

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  - 10 x 10G, 4 x 25G
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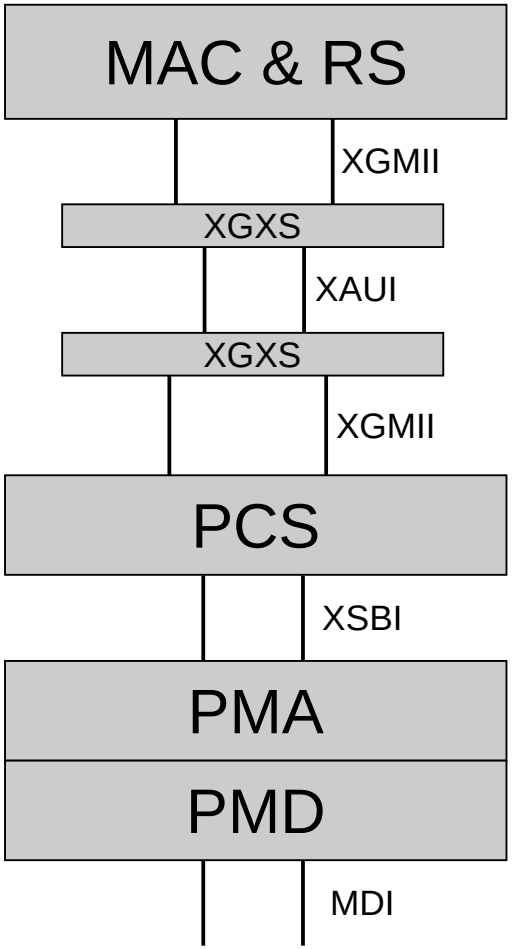
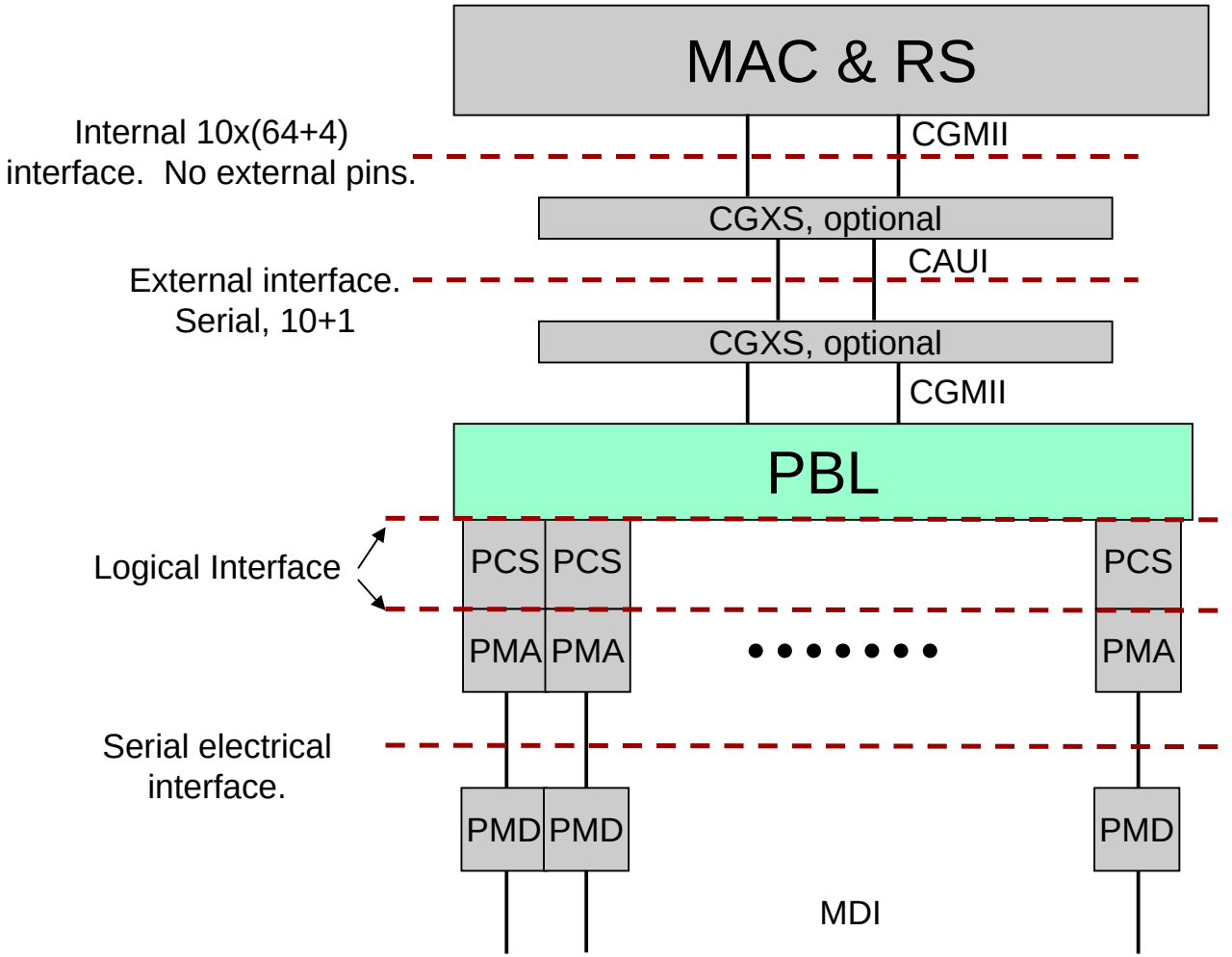
- **Summary**

PBL Model Architecture

- **Traditional 10GE**

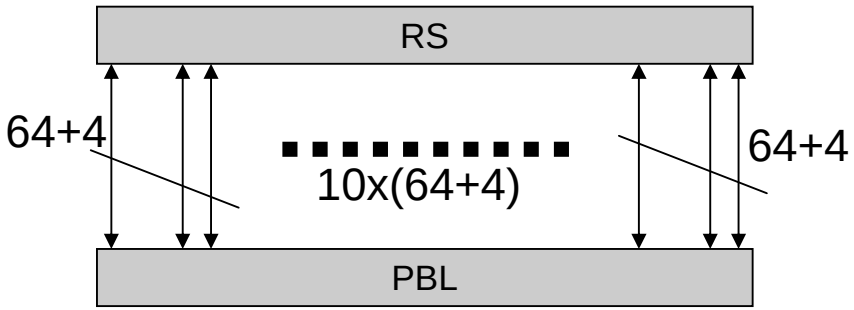


- **100GE Multi-Lane**

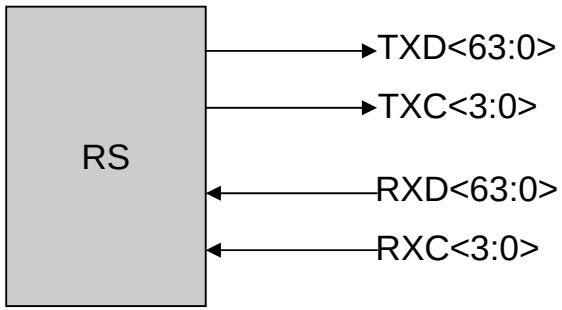


PBL Model Detail

CGMII interface



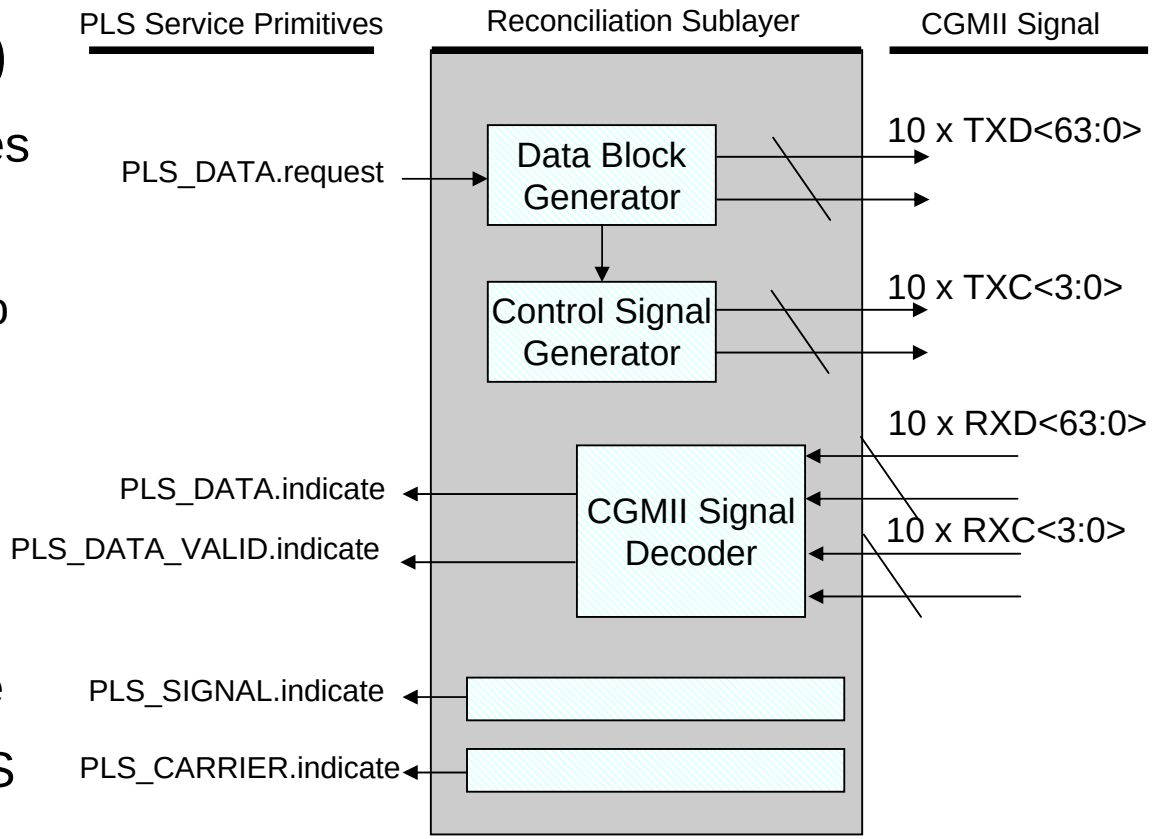
64+4 unit



- TXD and RXD: 64-bit data signal
- TXC and RXC: 4-bit control signal
- Clock: 156.25 Mhz, synchronized for all (64+4) units
- Speed:
  - Data Signal: 10 x 64 x 156.25 = 100 Gbps
  - Data Signal: 4 x 64 x 156.25 = 40 Gbps
- TXC and RXC to indicate the data block type

PBL Model Detail

- **RS (Reconciliation Sublayer)**
  - Mapping PLS service primitives signals to CGMII
    - Convert PLS request signal to 64bits data block
    - 10 x 64bits blocks generated parallel
    - Generate 4bits control signal according to 64bits block type
  - Mapping CGMII signals to PLS service primitives
    - Convert CGMII (64+4)bits signal to PLS service primitives



PBL Model Detail

- **Data block type**

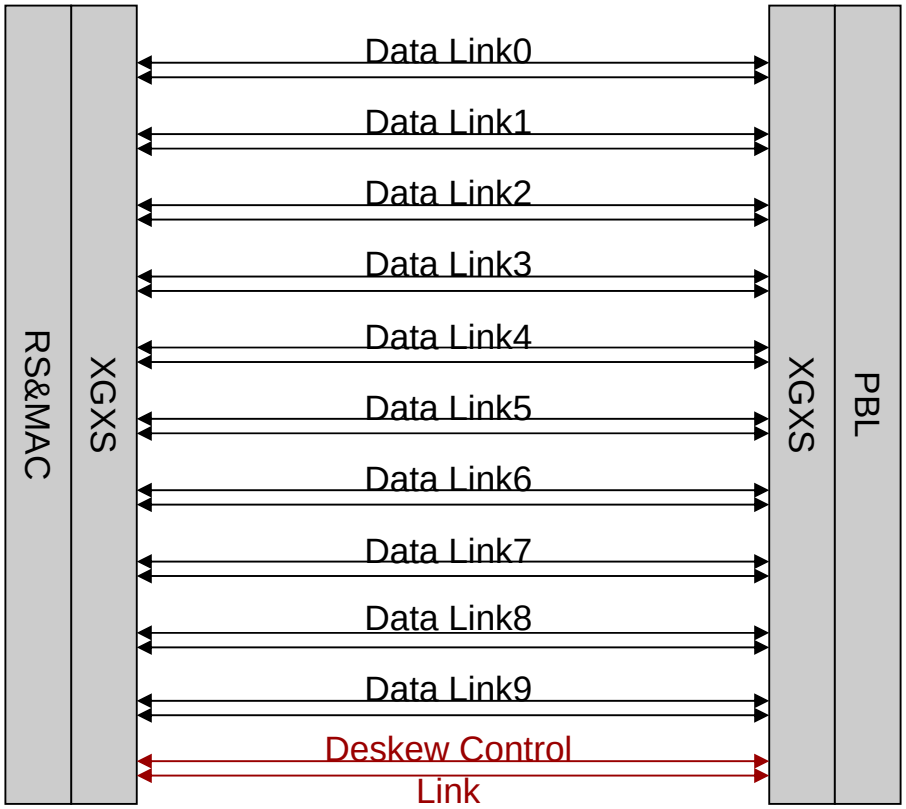
TXD/RXD								TXC/RXC	Description
D	D	D	D	D	D	D	D	0000	Data
S	D	D	D	D	D	D	D	1001	Start
C	C	C	C	S	D	D	D	1010	Start
T	C	C	C	C	C	C	C	1000	Terminate
D	T	C	C	C	C	C	C	0111	Terminate
D	D	T	C	C	C	C	C	0110	Terminate
D	D	D	T	C	C	C	C	0101	Terminate
D	D	D	D	T	C	C	C	0100	Terminate
D	D	D	D	D	T	C	C	0011	Terminate
D	D	D	D	D	D	T	C	0010	Terminate
D	D	D	D	D	D	D	T	0001	Terminate
C	C	C	C	C	C	C	C	1111	Control
A	A	A	A	A	A	A	A	New	Alignment
E	E	E	E	E	E	E	E	New	Error
N	N	N	N	N	N	N	N	New	Null
								Reserved	Order_set

PBL Model Detail

- **CAUI and CGXS**
  - CAUI: 100GE Attachment Unit Interface
    - External interface, for interconnection between chips
    - Can be used for Backplane interconnect
    - Optional interface
  - CGXS: 100GE Extender Sublayer
    - Converts signals from parallel CGMII to serial CAUI
    - Regenerate signal integrity after transmission on CAUI
    - Optional sublayer

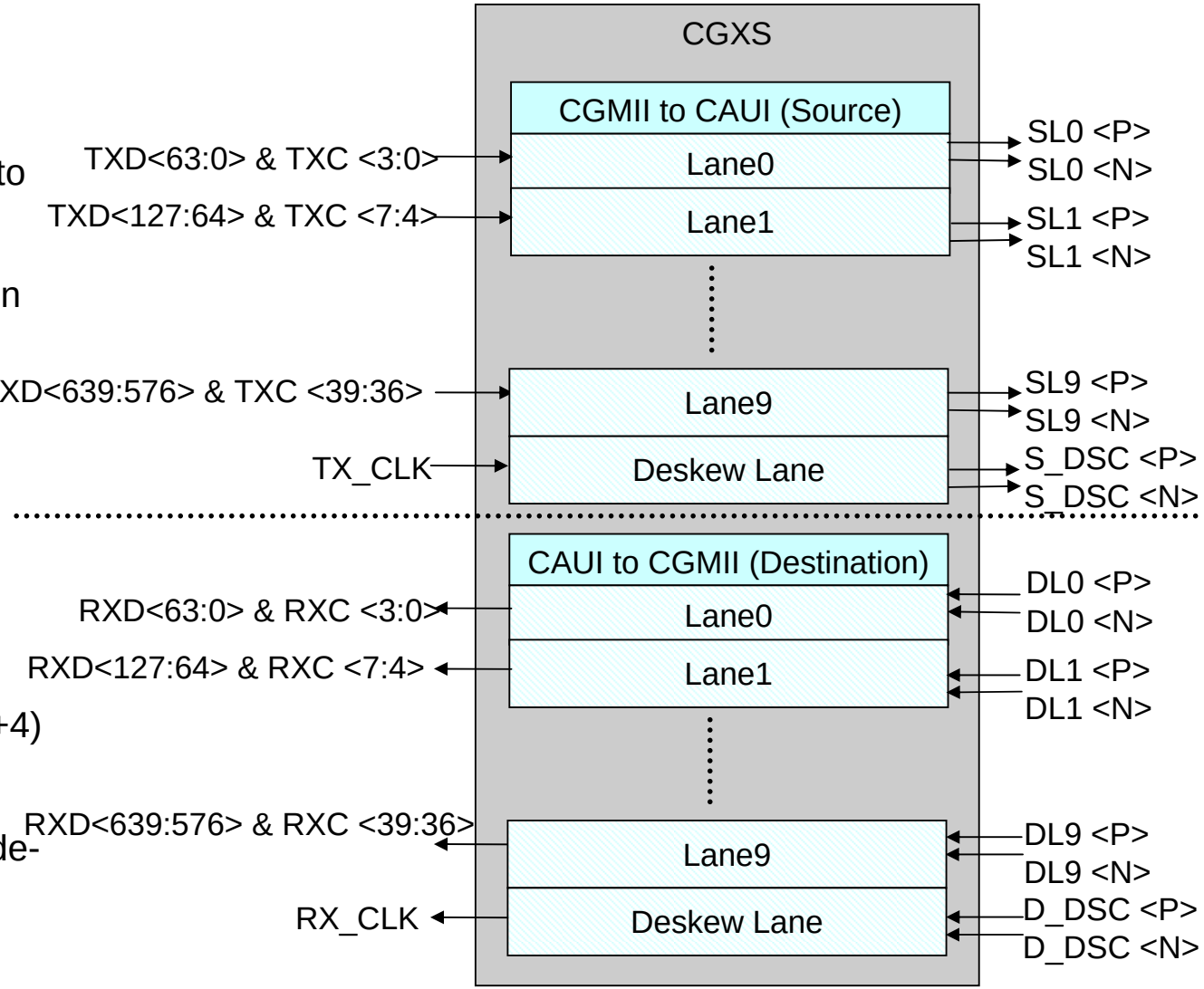
PBL Model Detail

- **CAUI**
  - 10 data + 1 deskew self-clocked serial differential links
  - 10.625Gbps per link



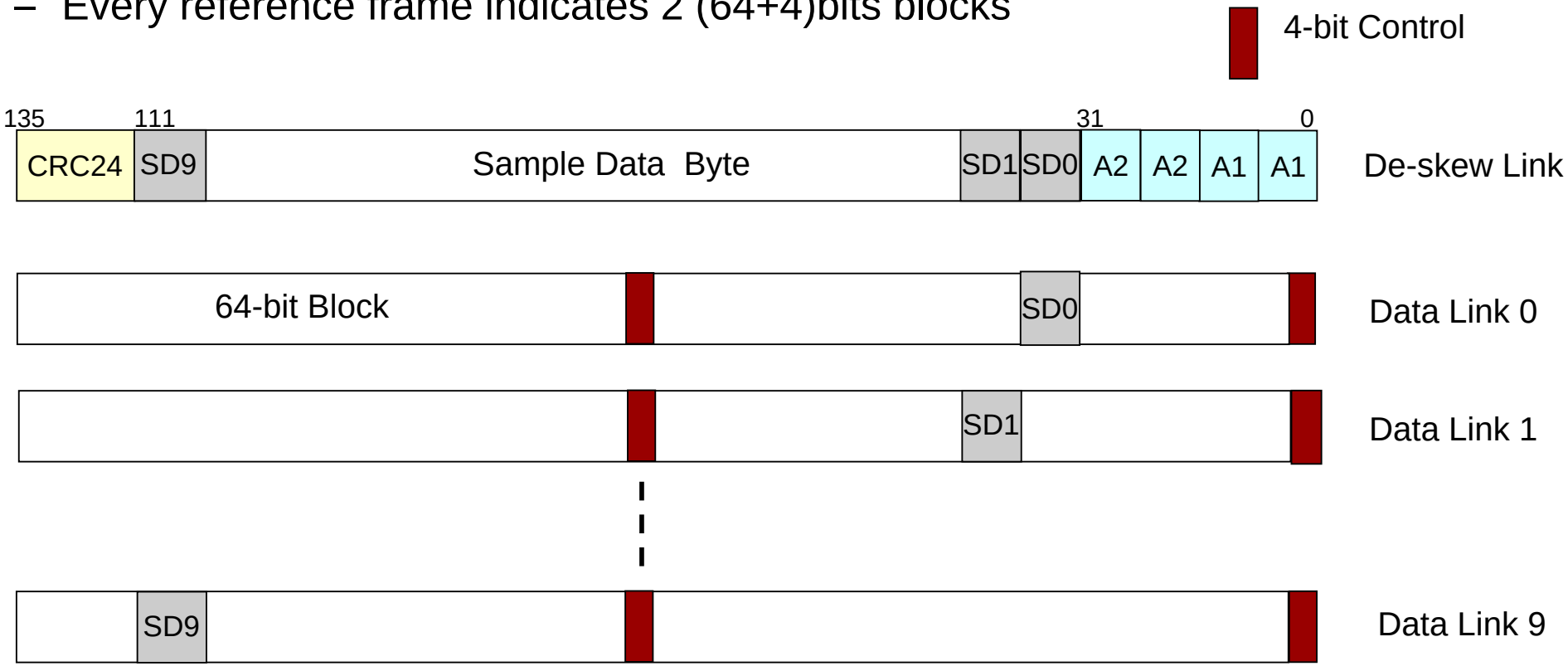
PBL Model Detail

- **CGXS**
  - From CGMII to CAUI
    - Mux (64+4) parallel signals to serial on every lane
    - Generate de-skew signals on de-skew lane
    - Scramble before serial transmission
  - From CAUI to CGMII
    - Recover clock signal
    - Descramble
    - Demux serial signals to (64+4) parallel on every lane
    - Align parallel signals using de-skew information
    - Output CGMII signals



PBL Model Detail

- **How to generate the de-skew control signal at CGXS**
  - Reference Frame: 136 bits in length
    - A1&A2: Framing byte. Also indicates the beginning of 2x (64+4)bits blocks
    - SD: Sample Data byte, Sampling 8bits from each link in order
    - CRC24: For Reference Frame error checking
  - Every reference frame indicates 2 (64+4)bits blocks



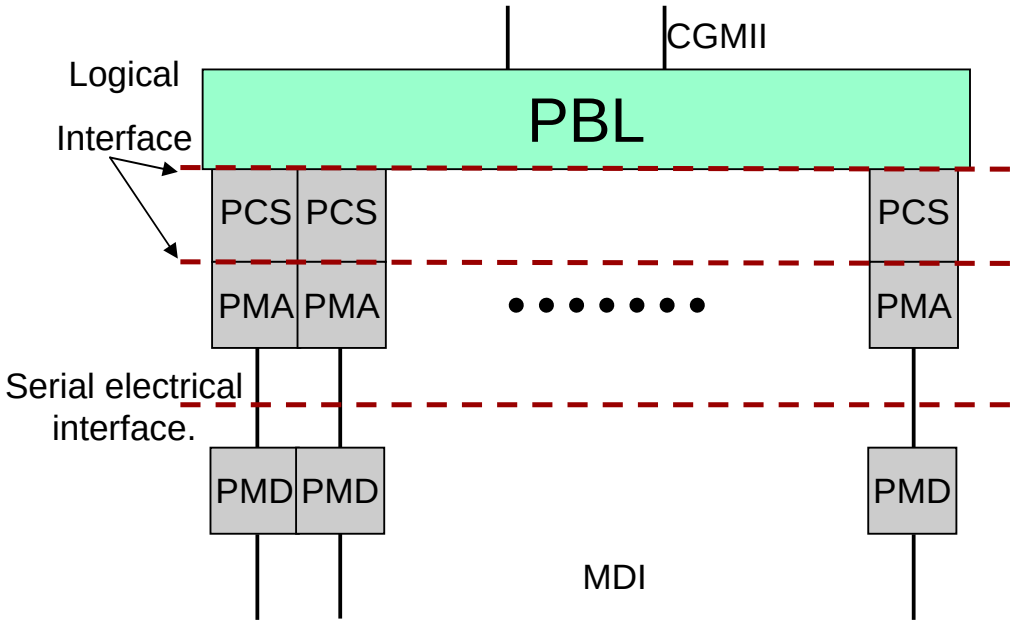
PBL Model Detail

- **Signal re-alignment at CGXS**
  - Determine reference frame start by recovering A1A1A2A2 framing
  - Search SD0~SD9 at each corresponding data link to determine the skew
  - Reassemble CGMII signal after de-skewing each lane
  - Each reference frame delineates 136-bit blocks [2x(64+4)]

- **Scramble/Descramble at CAUI**
  - Scramble/descramble each lane independently to keep DC balance when transmitting on CAUI
  - Reuse 10GE scrambler polynomial: $X^{58} + X^{39} + 1$

PBL Model Detail

- **Other interfaces of PBL layer model**
  - Interfaces between PBL/PCS/PMA
    - Logical only, not external
  - Interface between PMA and PMD
    - External serial electrical interface
    - Based on 64b/66b data blocks
    - 10 x 10Gbps for 10 PMDs (XFI, etc.)
    - 4 x 25Gbps (CEI-25, etc.) for 4 PMDs, 2 PMDs or Serial PMD
    - Keep optical module stand-alone
    - Interconnect with other module, such as OTN mapping

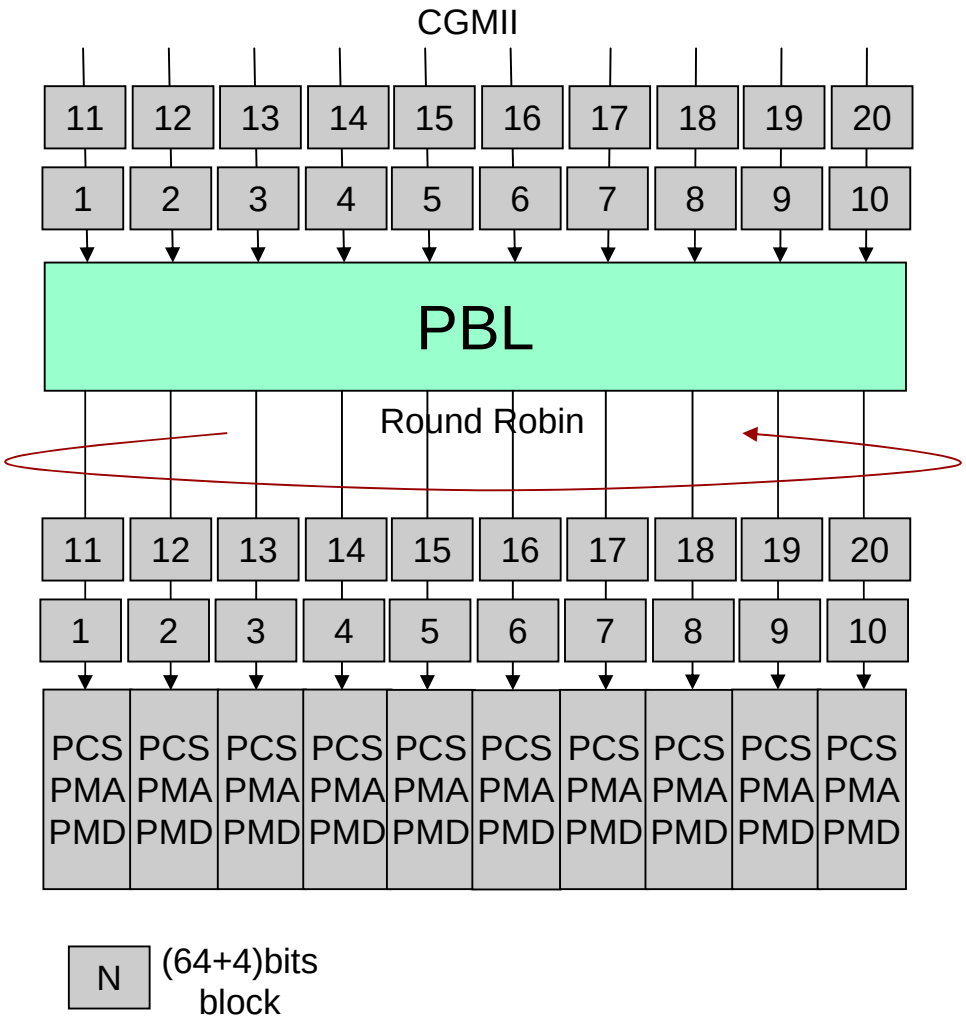


PBL Function

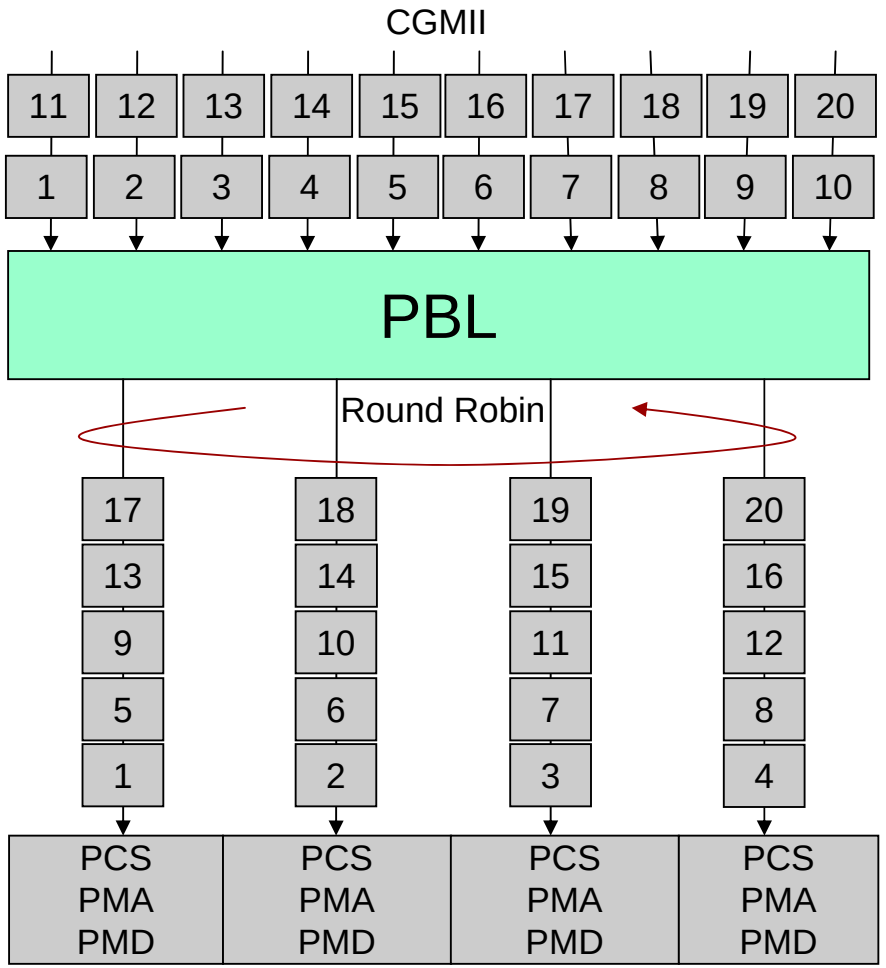
- **Block Distribution**
  - Based on 64-bit blocks, to correspond with 64b/66b coding at PCS
  - Uniform distribution and reassembly method for different number of lanes using round robin method
- **Alignment**
  - Insert alignment blocks at transmitter
  - realign received data using alignment blocks

PBL Function

- **Block Distribution – 10 Lanes**

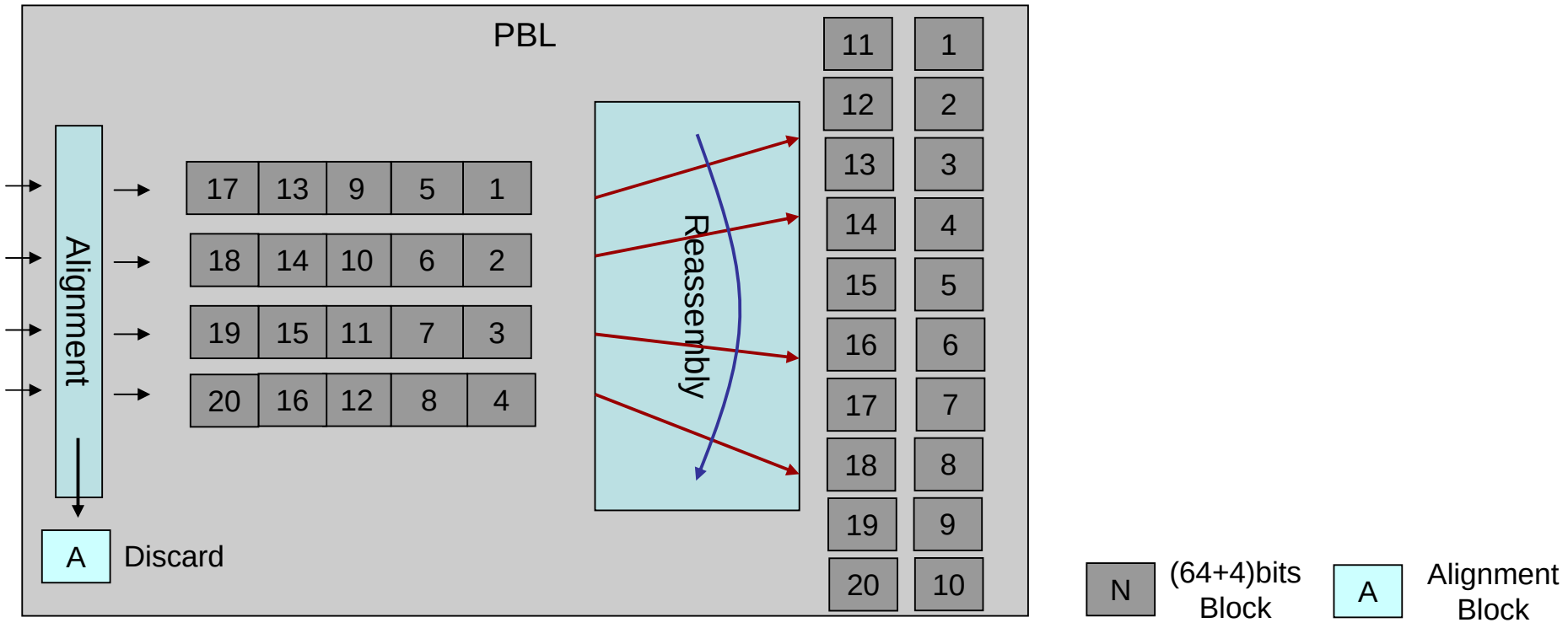


- **Block Distribution – 4 Lanes**



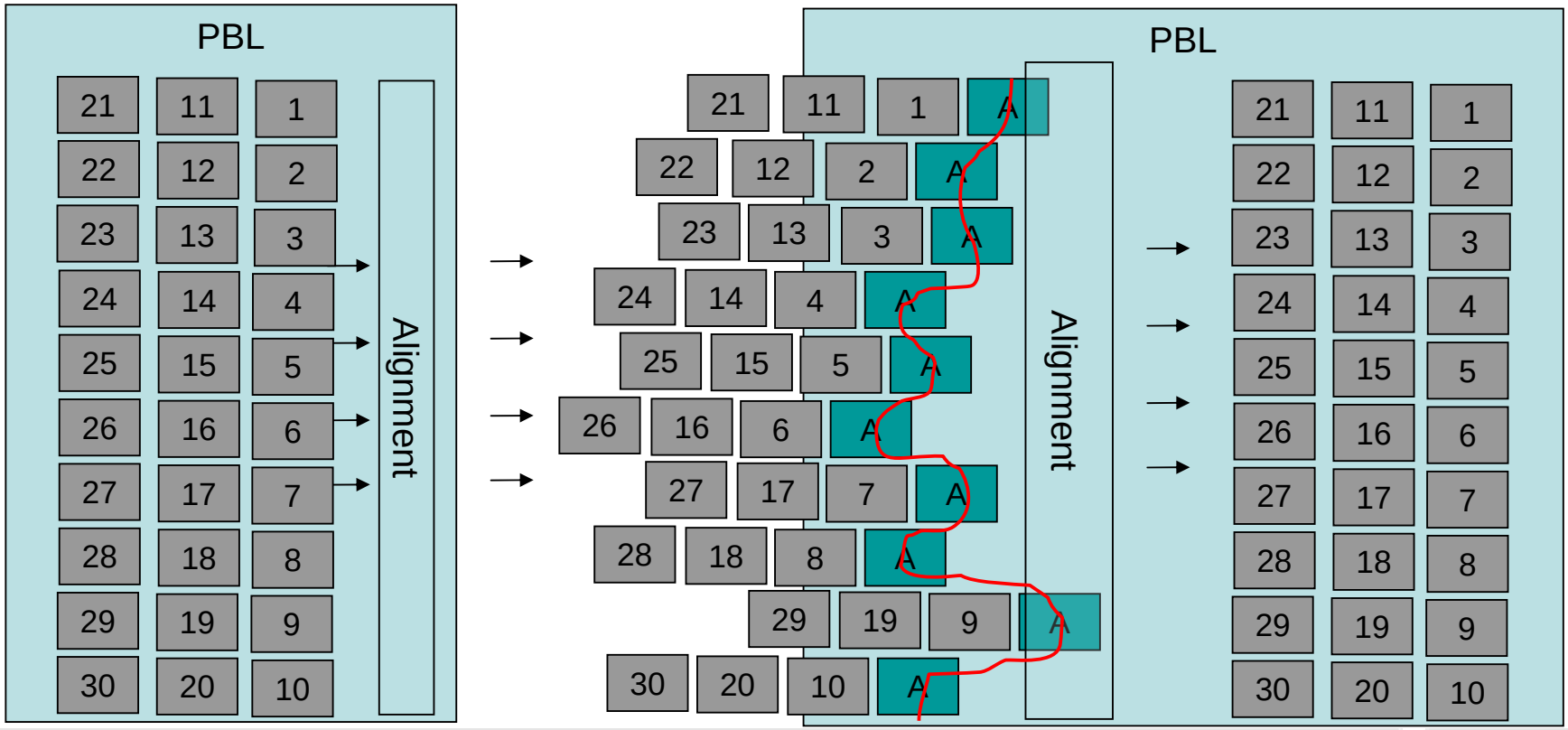
PBL Function

- **Block reassembling**
  - All received data blocks from different lanes are aligned at PBL
  - Aligned data blocks are reassembled to form CGMII data by round robin



PBL Function

- **Alignment at PBL**
  - PBL inserts alignment block at the same time for all lanes when needed
    - Alignment block is a special 64-bit control block
  - At receiver, PBL searches for alignment blocks to determine the lane de-skew and align each lane's data blocks



PBL Function

- **Alignment with fault lanes**
  - At transmitter
    - Alignment blocks are inserted into all lanes, regardless of fault status. Data on fault lanes is NULL control blocks.
  - At receiver
    - Alignment and data recovery is performed on available lanes, data on failed lanes is not used by reassembly block
    - After faulty lane has recovered,
      - Alignment is performed on the recovered lane,
      - Data is recovered and used by reassembly block

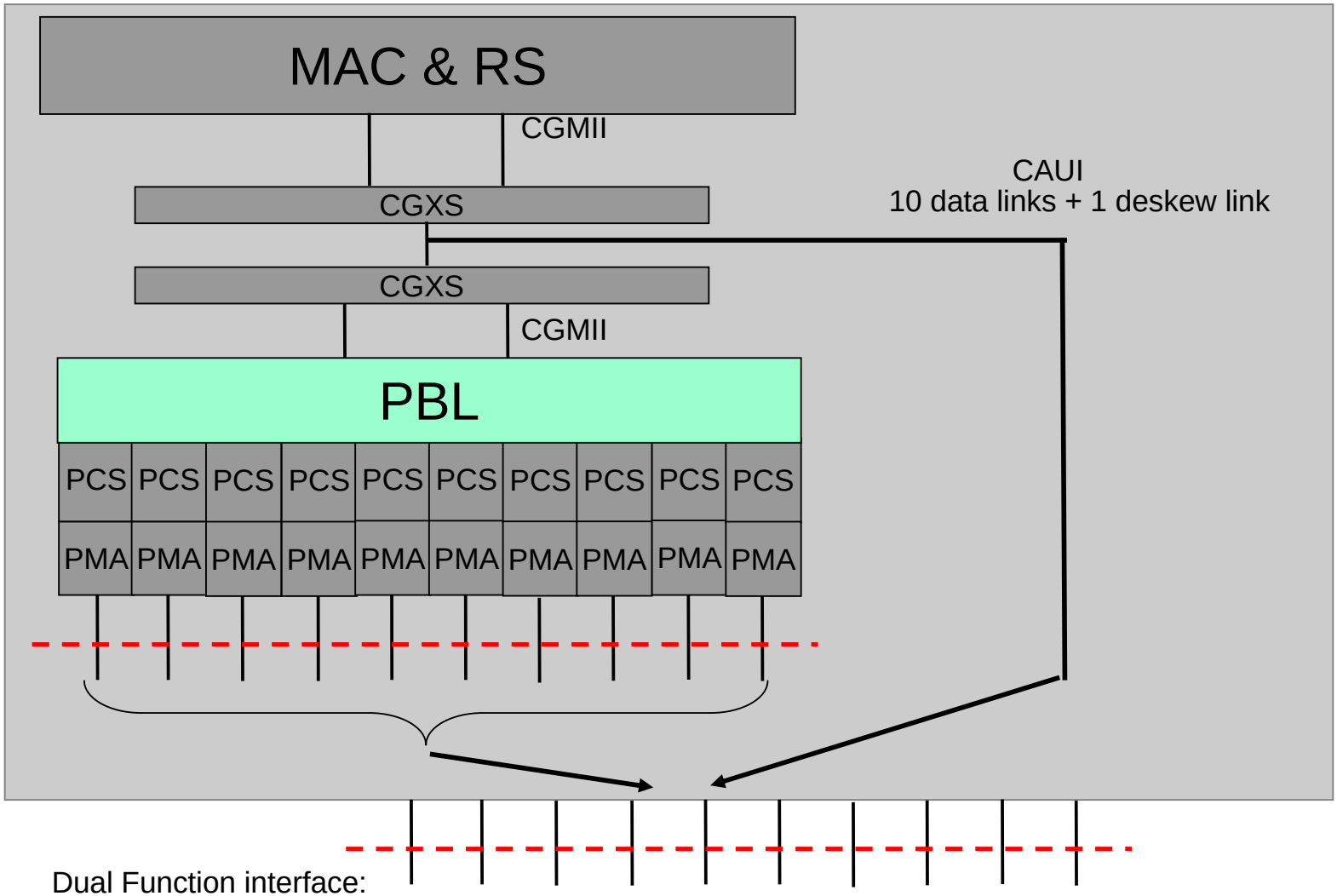
PBL Function

- **Bandwidth for alignment blocks**
  - In-band
    - Insert alignment blocks when needed
    - Delete following IPG to compensate the bandwidth occupied by alignment blocks
    - Trigger for sending of alignment blocks can be periodic (interrupt a packet) or the end of a packet (do not interrupt a packet)
    - With either trigger, insertion interval needs to be long enough to guarantee effective IPG compensation.
    - Recover IPG at receiver PBL, to keep IDLE bytes >= 12 per packet
  - Out-of-band
    - Increase the line rate to get the additional bandwidth for alignment blocks
    - Insert alignment blocks periodically

PCS Function

- **Concerns about per-lane scrambling and error propagation**
  - Use a frame synchronous scrambler similar to SONET/SDH
    - Scrambler is additive rather than multiplicative so no error multiplication occurs in the receiver
    - Scrambler reset would occur on each alignment block
    - The same X^7 polynomial from SONET could be used
    - Malicious data causing scrambler problems is unlikely due to
      - Data is spread across 4 or 10 lanes; MAC data will be unaware which data bytes will land on which lanes
      - MAC data will be unaware of scrambler reset interval (when alignment blocks are generated/removed)

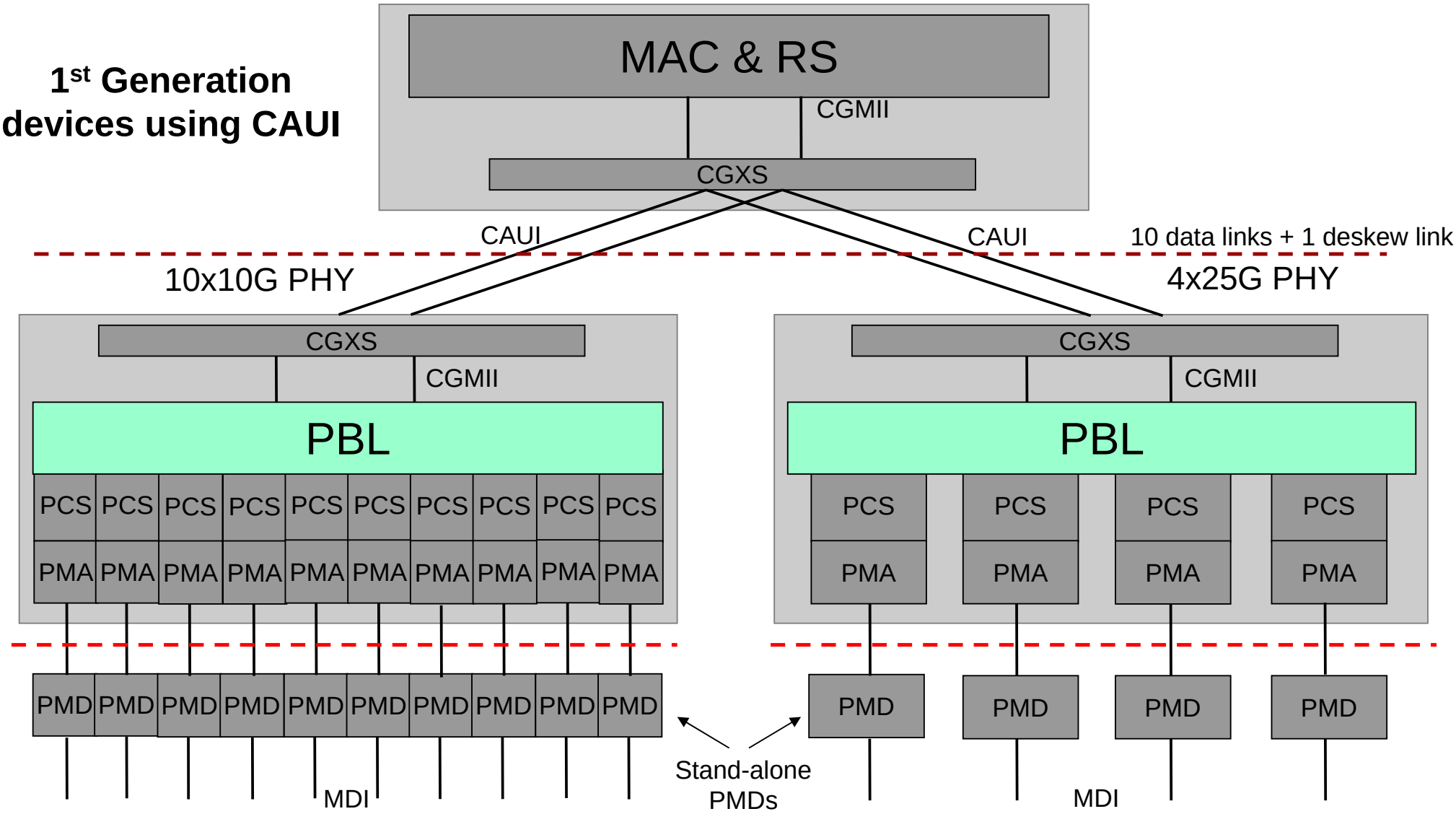
PBL Layer Model Application



Dual Function interface:
A: 10 data links + 1 deskew link for CAUI, or
B: 10 serial lanes for PMA connection

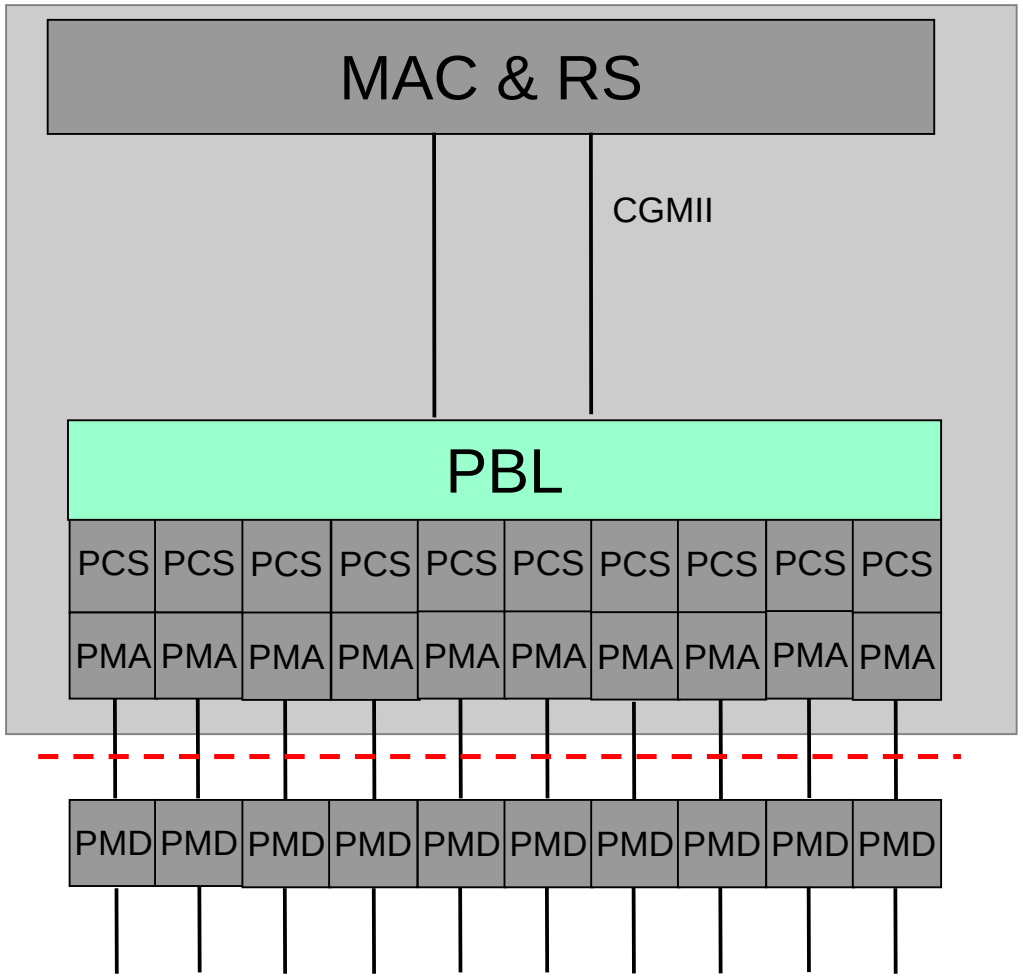
PBL Layer Model Application

1st Generation devices using CAUI



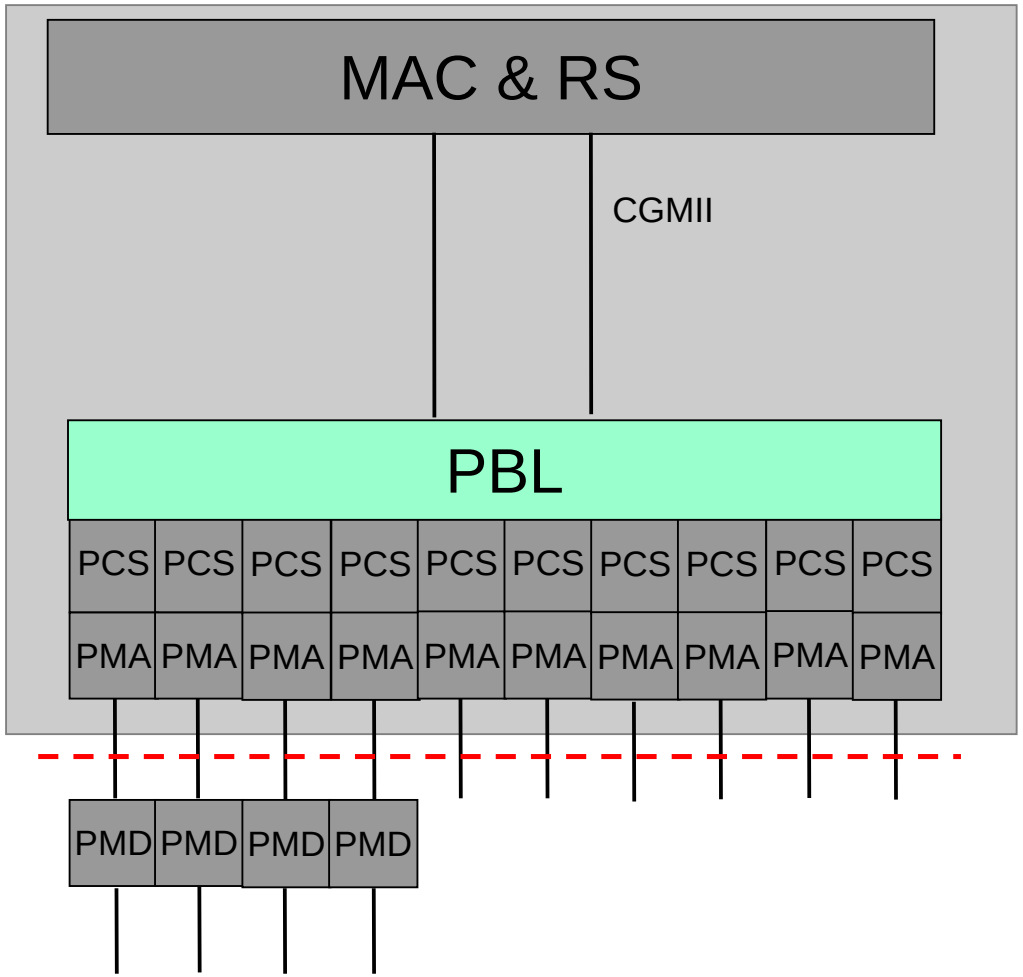
PBL Layer Model Application

1st Generation devices using PMA interface for 10 lanes



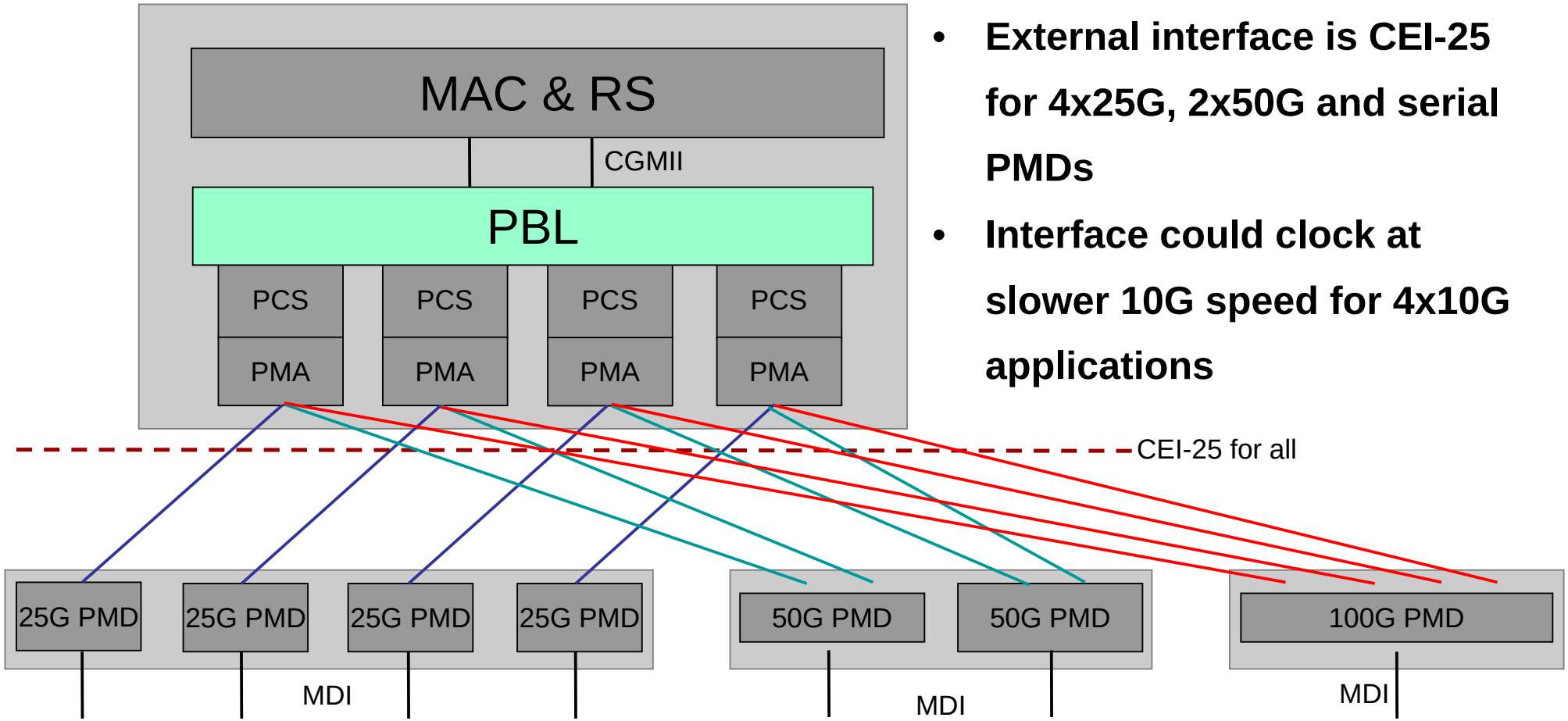
PBL Layer Model Application

- **1st Generation devices using PMA interface for 4 lanes**
- **PBL is programmable to distribute data to 4 or 10 lanes**



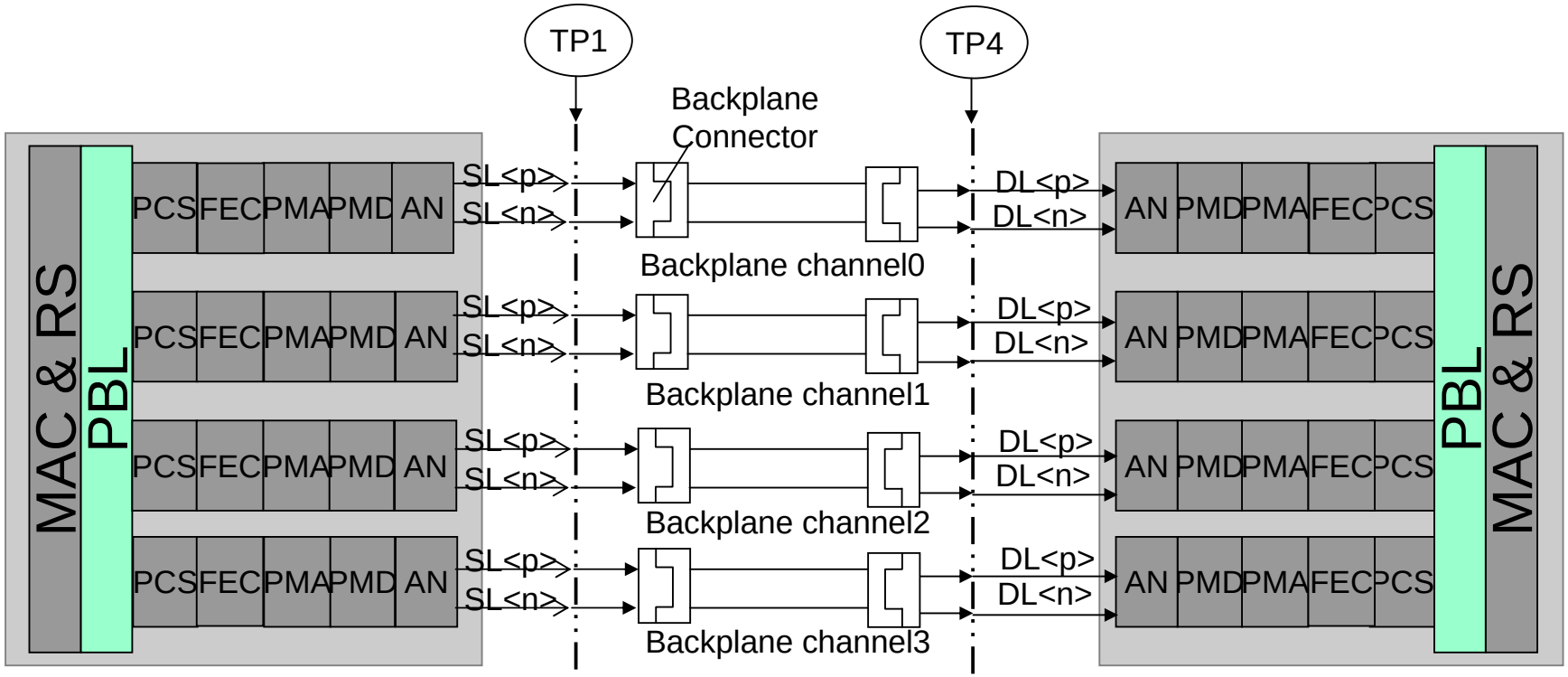
PBL Layer Model Application

- **MAC and PHY integrated together (2nd generation)**
- **External interface is CEI-25 for 4x25G, 2x50G and serial PMDs**
- **Interface could clock at slower 10G speed for 4x10G applications**



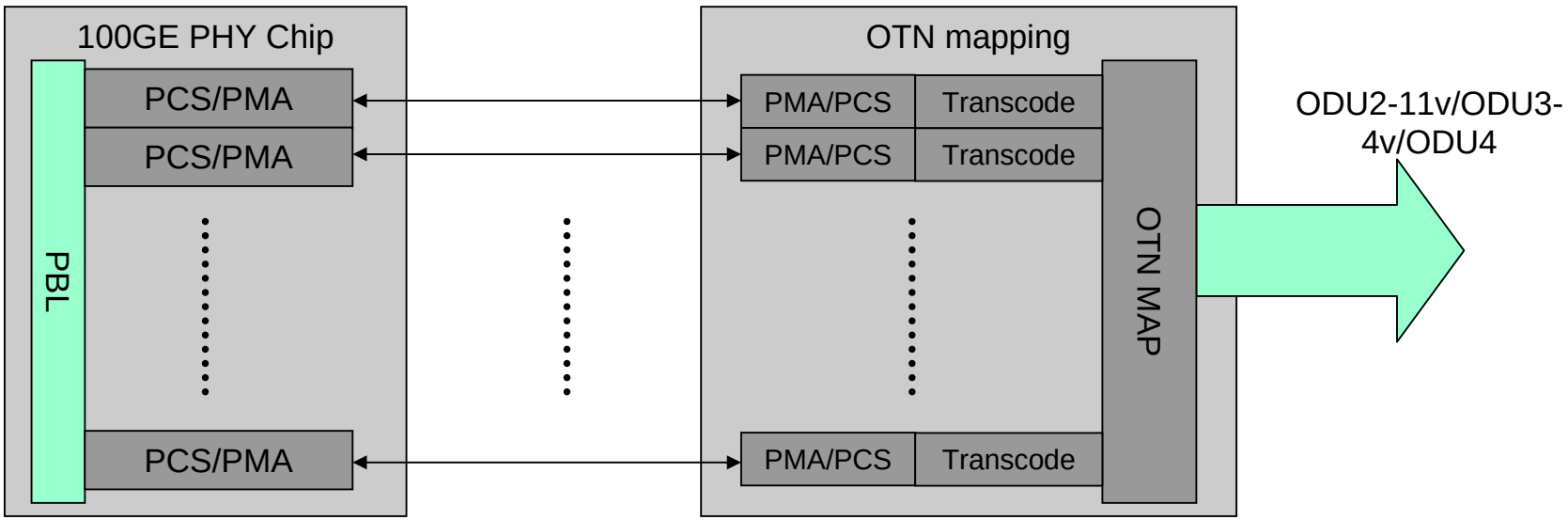
PBL Layer Model Application

- **Backplane application**
  - Easy to reuse 802.3ap, clause 72, 73 and 74
  - Flexibly expand from 4x10GE to 10x10GE
  - Lane FEC can reduce impact of error propagation



PBL Layer Model Application

- **Compatible with OTN**
  - With a block interface between PMA and PMD, interconnection with OTN mapping modules is simplified
  - No special requirements for traditional OTN mapping modules
  - Easy to map 100GE into ODU2/ODU3 with virtual concatenation (VCAT) and Link Capacity Adjustment Scheme (LCAS) or single ODU4



Summary

- **New CAUI and CGXS**
  - To extend the CGMII and provide an external interface
  - Support 10x10Gbps or 4x25Gbps PHYs
- **Detail information about PBL function**
  - Block distribution and reassembly to adapt different numbers of lanes at PBL
  - Multi-Lane alignment scheme
  - Introduction of synchronous scrambling idea
- **Advantage of PBL model**
  - More suitable for backplane application
  - Block interface, easy to interconnect with OTN mapping module

Thank You

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