Photonic Integration Considerations for the 100GbE SMF PHYs

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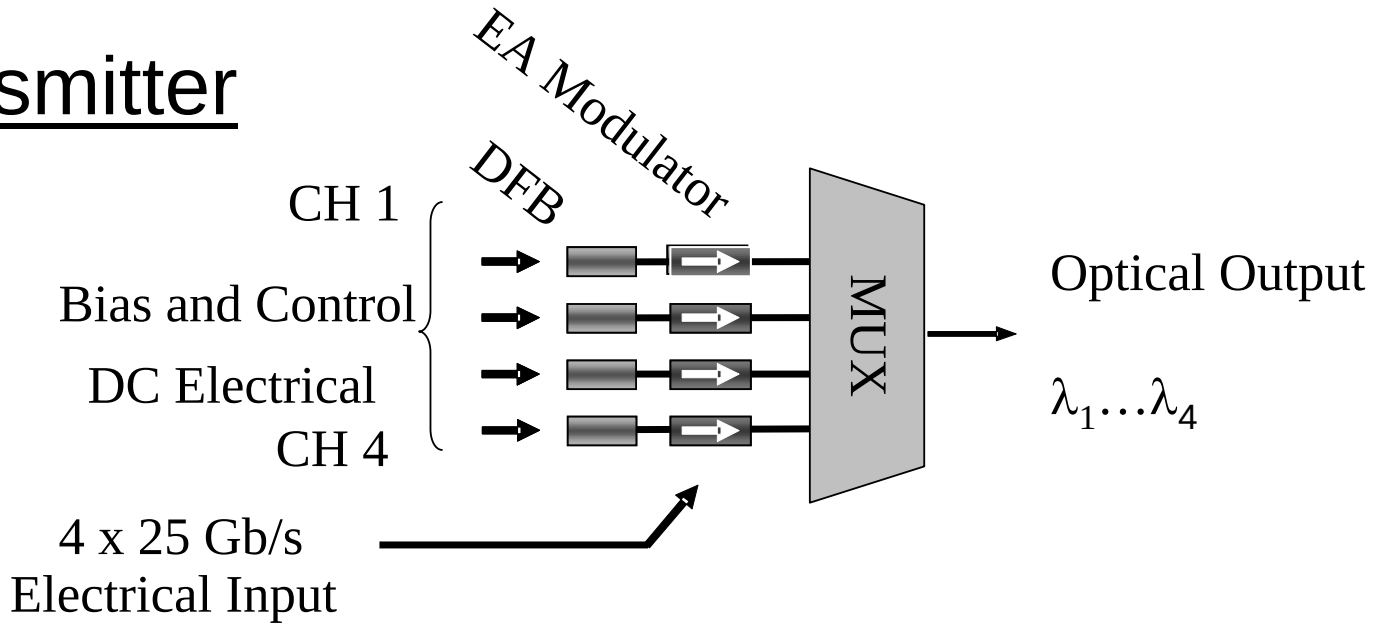
Key Considerations For 100GbE Monolithic Integration

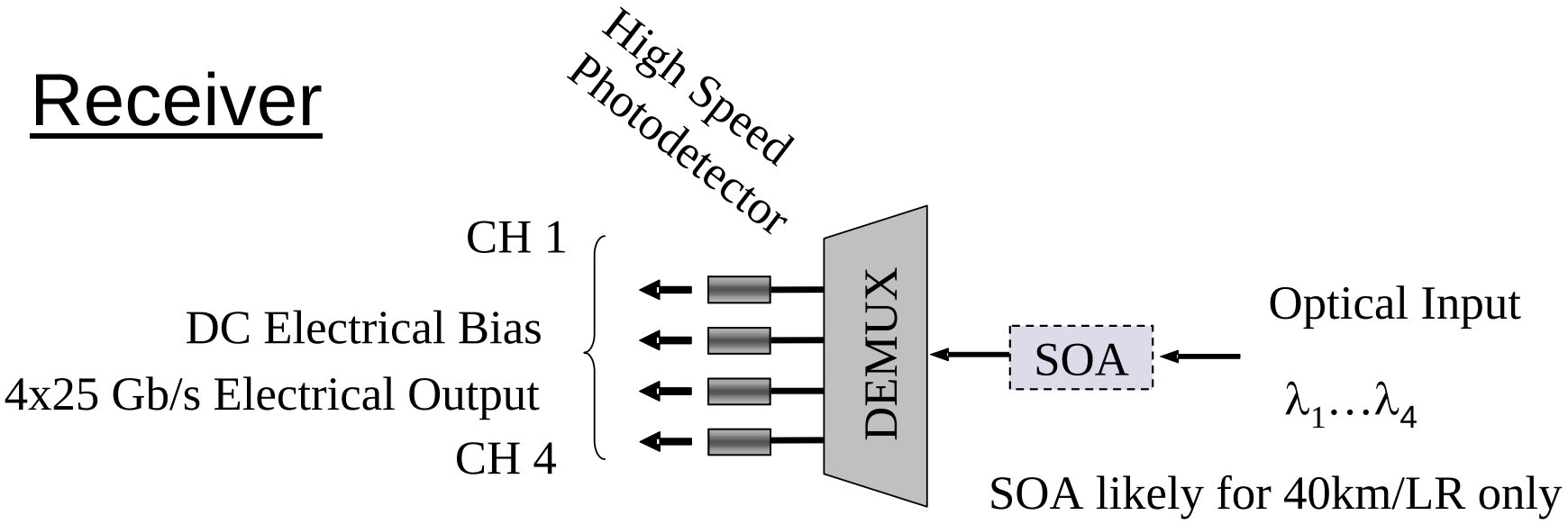
- Range of Active Wavelengths (material bandgaps) Required on a Chip
- Wavelength Accuracy / Drift Requirements
- Modulator Performance
- Designs for Longer Reaches (e.g. 40km)

100GbE – Potential Integrated Architectures

Transmitter



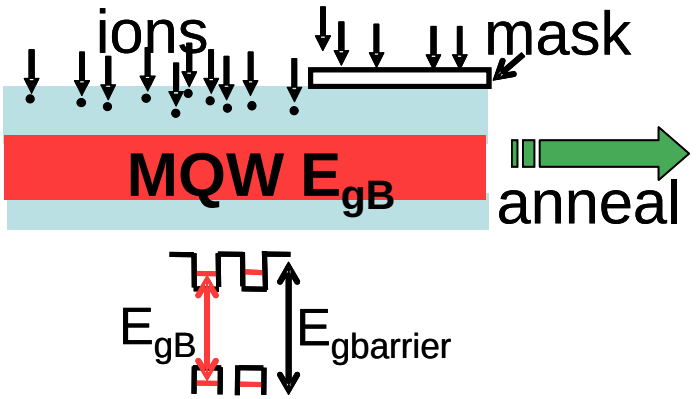
Receiver

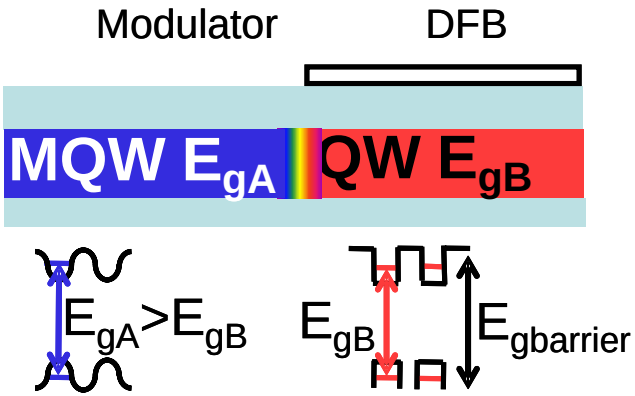


Range of Active Wavelengths (Bandgaps) Required on Chip

- Prefer narrower channel spacings (200 - 400GHz);
- Requires less bandgap tuning than CWDM (20nm) for commonly used fabrication techniques and is more compatible with a variety of monolithic integration techniques
  - 4 channels at 25Gbit/s each at a channel spacing of 400GHz (400 x 3 = 1200GHz or ~10nm)
  - Typical bandgap detunings between modulator and DFB are ~30-60nm
  - Total bandgap range span on a 4x 25Gbit/s EML array is:
    - ~40-70nm for 400GHz spacing
    - ~90-120nm for 20nm channel spacing
  - A 40-70 nm range of active wavelengths allows a number of low cost, high volume production technologies for band gap engineering
    - Impurity induced layer disordering; selective area growth; and re-growth for production of the laser modulator array on a single chip
  - Larger wavelength (e.g., CWDM) ranges are more complex/costly
    - Larger ranges push the limit of integration technologies such as impurity induced layer disordering and selective area growth and require more epi calibrations for integration via re-growth

Bandgap Tuning Via Impurity Induced Layer Disordering





- To achieve low cost – simple, high yield processes are required
- >40 nm band gap shift (400GHz channel spacing) for optimal performance can be achieved within a wide range of parameters
- >90nm bandgap shift (20nm channel spacing) pushes the limit of the technology and likely results in higher manufacturing costs

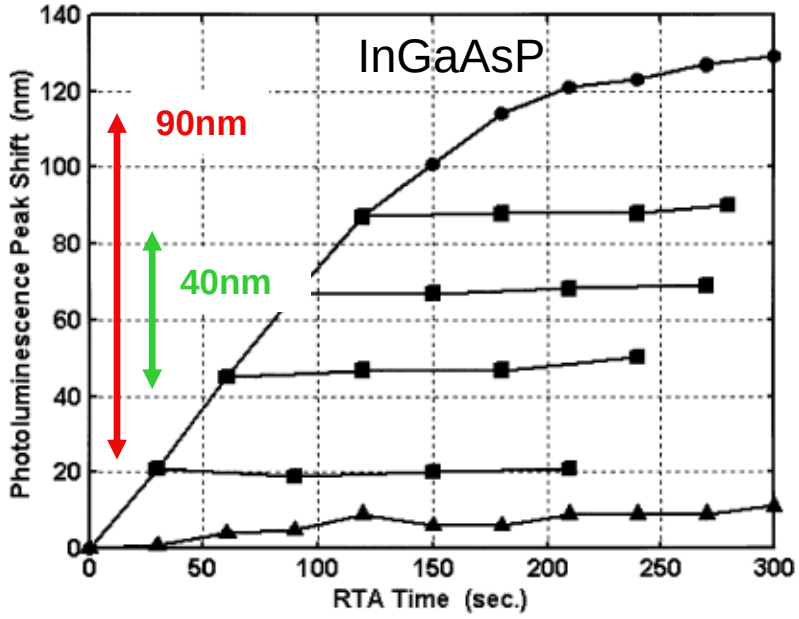
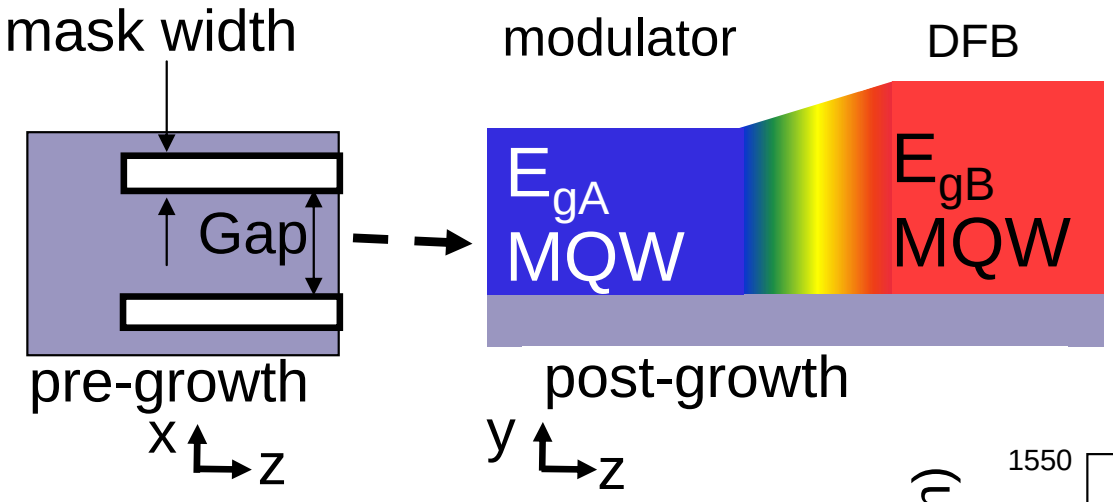


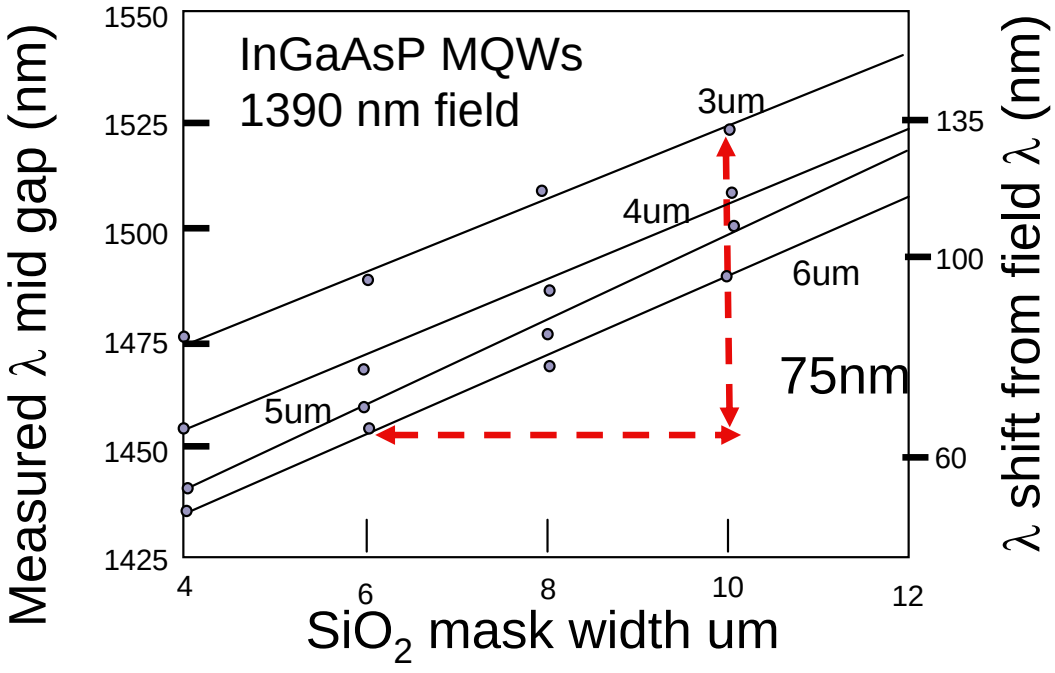
Fig. 3. Peak photoluminescence peak shift as a function of anneal time, showing the initial linear increase in the peak shift and the complete halting of the peak shift for samples for which the implant buffer layer has been etched. Symbols indicate nonimplanted (triangles), implanted (circles), and samples with partial anneal followed by the removal of the implant buffer layer (squares).

IEEE JOURNAL OF SELECTED TOPICS IN QUANTUM ELECTRONICS, VOL. 9, NO. 5, SEPTEMBER/OCTOBER 2003 1183
Erik J. Skogen, *Student Member, IEEE*, James W. Raring, Jonathon S. Barton, *Student Member, IEEE*,
Steven P. DenBaars, *Member, IEEE*, and Larry A. Coldren, *Fellow, IEEE*

Bandgap Tuning Via Selective Area Growth



- Large bandgap tuning shifts require increasing complexity in mask design, and additional cost in epi calibration, and material characterization
- Practically, 40nm shift much easier to control / reproduce than 90nm shift



C. H. Joyner, **S.** Chandrasekhar, J. W. Sulhoff. and **A.** G. Dentai
IEEE PHOT TECH LETT, VOL. 4, NO. 9, SEPTEMBER 1992

Wavelength Accuracy / Drift Requirements

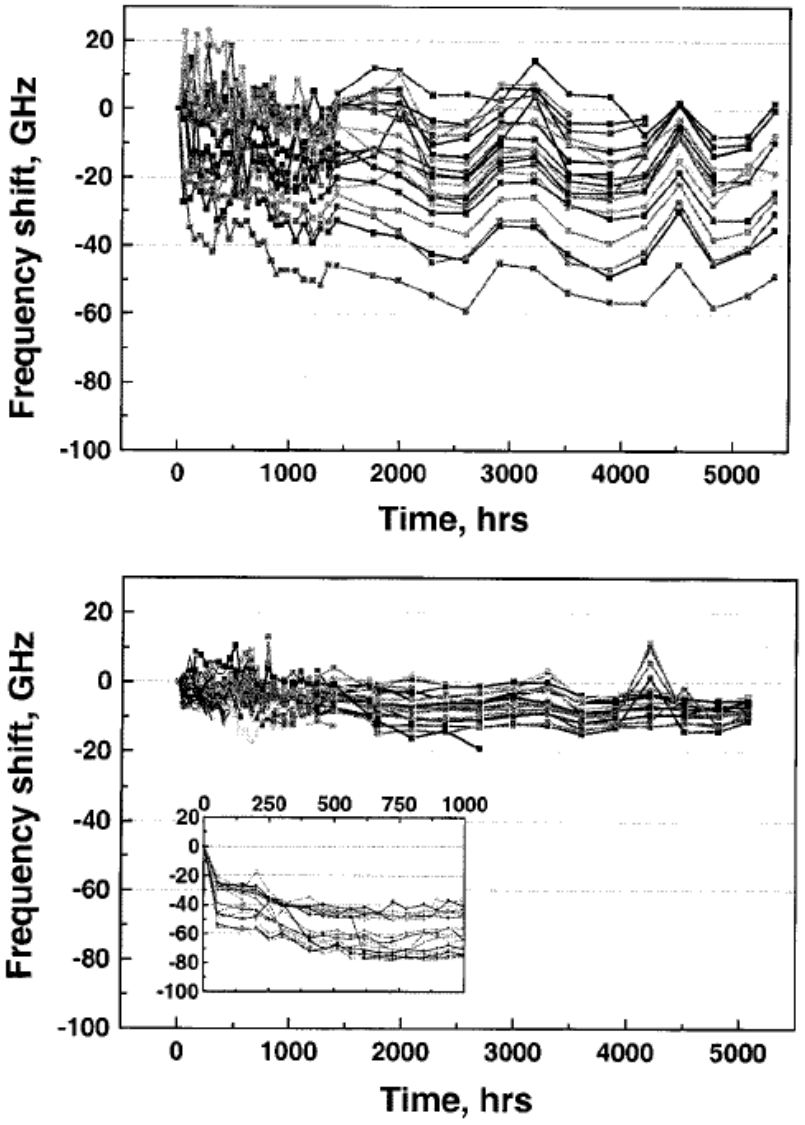


Fig. 4. Normalized frequency drift for (a) device with 37 hours burn-in and (b) 600 hours burn-in. The inset shows enlarged scale frequency shift for the first 1000 hours of the operation time.

400GHz preferred to 200GHz for reduced BoL accuracy and more range for EoL

- 400GHz grid provides more room for DFB wavelength shift; reduces cost by reducing the need for BoL targeting; and relaxes EoL wavelength shift requirements
- Reduced BoL targeting requirements result in higher yield (less accuracy required in epi and fab processes)
- Reduced EoL wavelength shift requirements reduce need for Burn-In
  - Burn-in of typical InP based transmitters can significantly reduce frequency drift over life, but is costly in terms of time and test
  - +/-400pm (50GHz) after 5000 hours of stress (HTSL at 85ºC or HTOL at 50ºC/70mA) is typical
  - A 400GHz operation window allows a comfortable margin to reduce cost by eliminating or reducing the need for Burn-In

J. LIGHTWAVE TECH, VOL. 18, NO. 12, Dec 2000, p.2196.
Olga A. Lavrova, and Daniel J. Blumenthal,

Channel Spacing and Chromatic Dispersion

- Using ITU-T G.652 Standard (06/2005), chromatic dispersion in the standard SMF is given by the following relationship.

$$\frac{\lambda S_{0\max}}{4}\left[1-\left(\frac{\lambda_{0\max}}{\lambda}\right)^4\right] \le D(\lambda) \le \frac{\lambda S_{0\max}}{4}\left[1-\left(\frac{\lambda_{0\min}}{\lambda}\right)^4\right]$$

Chromatic dispersion coefficient	$\lambda_{0\min}$	1300 nm
	$\lambda_{0\max}$	1324 nm
	$S_{0\max}$	0.092 ps/nm^2 × km

- Using this you can construct an ITU-like grid in the 1300nm to 1324nm region which is pegged to the ITU grid in the C band (1550nm region) at 100GHz intervals.

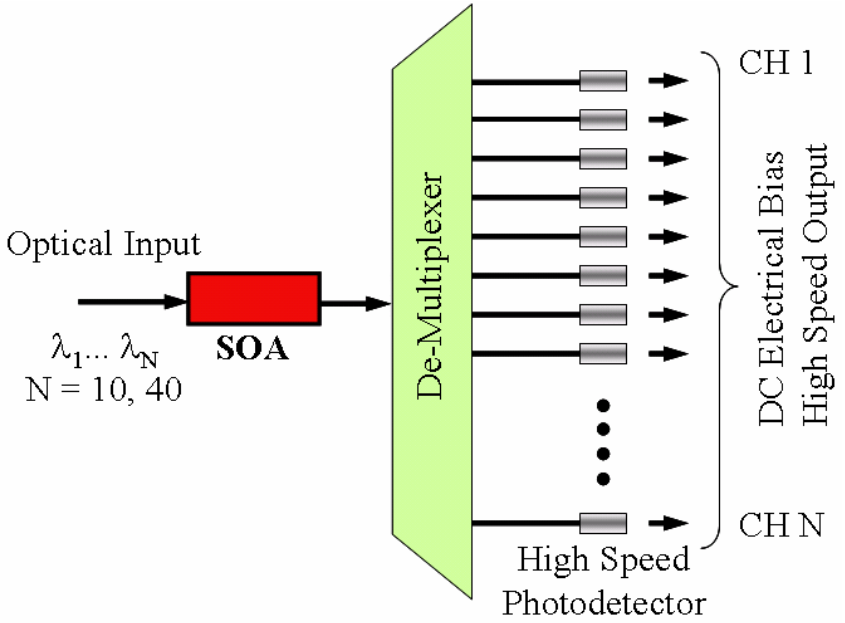
200GHz Channel Spacing Proposal				
Channel	Wavelength (nm)	Frequency (GHz)	DispersionMin, ps/nm	DispersionMax, ps/nm
1	1310.282	228800	-1.28	0.93
2	1311.428	228600	-1.17	1.04
3	1312.576	228400	-1.06	1.14
4	1313.727	228200	-0.96	1.24

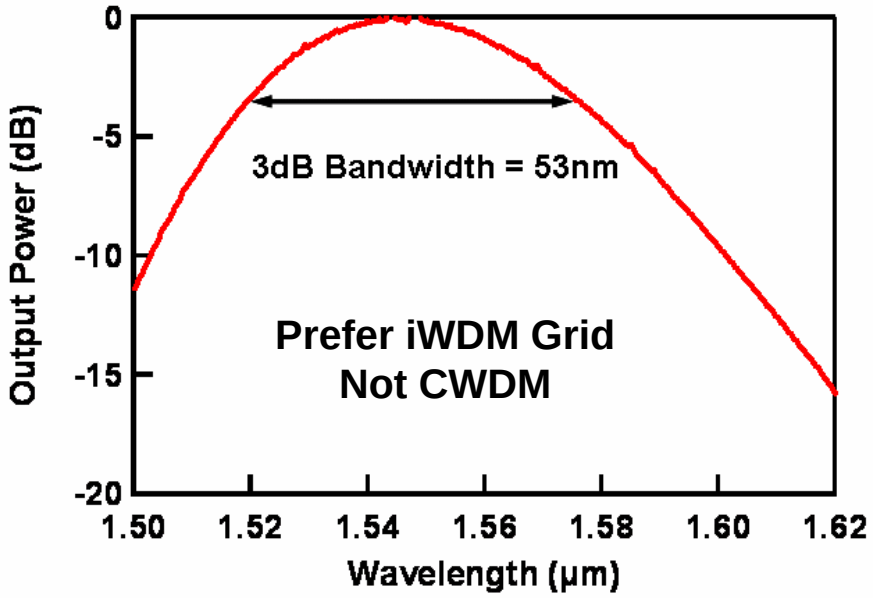
400GHz Channel Spacing Proposal				
Channel	Wavelength (nm)	Frequency (GHz)	DispersionMin, ps/nm	DispersionMax, ps/nm
1	1308.566	229100	-1.45	0.78
2	1310.855	228700	-1.23	0.99
3	1313.151	228300	-1.01	1.19
4	1315.456	227900	-0.79	1.40

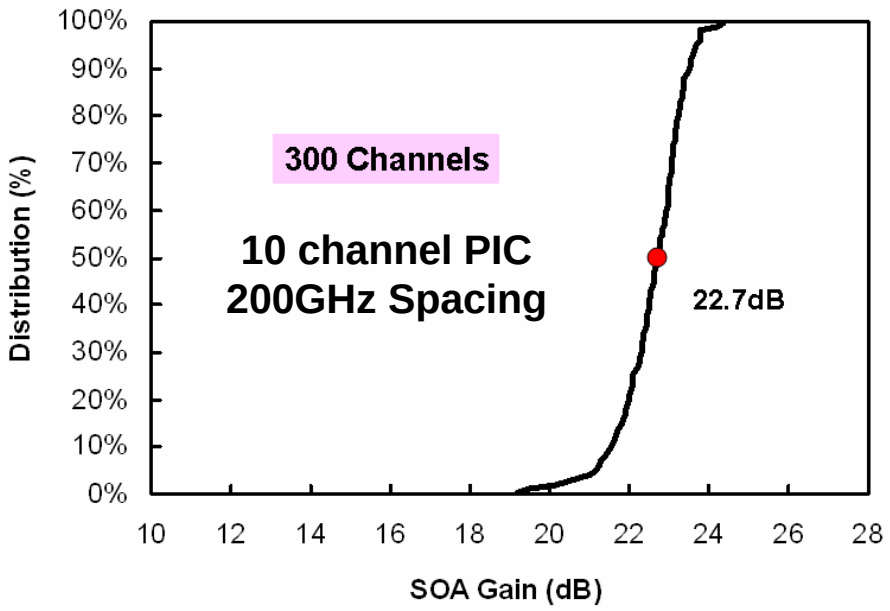
800GHz Channel Spacing Proposal				
Channel	Wavelength (nm)	Frequency (GHz)	DispersionMin, ps/nm	DispersionMax, ps/nm
1	1305.148	229700	-1.77	0.47
2	1309.709	228900	-1.34	0.88
3	1314.303	228100	-0.90	1.29
4	1318.929	227300	-0.47	1.70

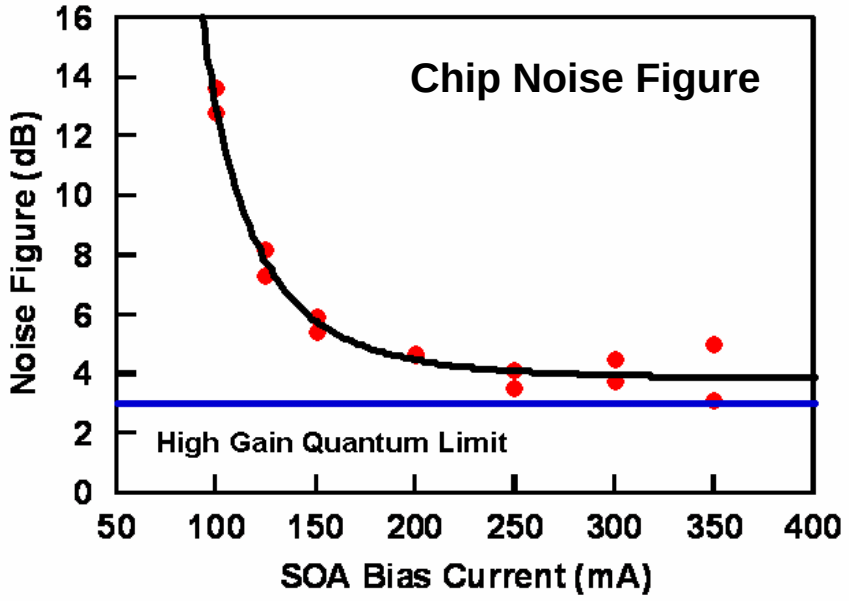
Fiber chromatic dispersion considerations for 40km PHY favor a narrower channel spacing

Infinera SOA Integrated Receiver PIC

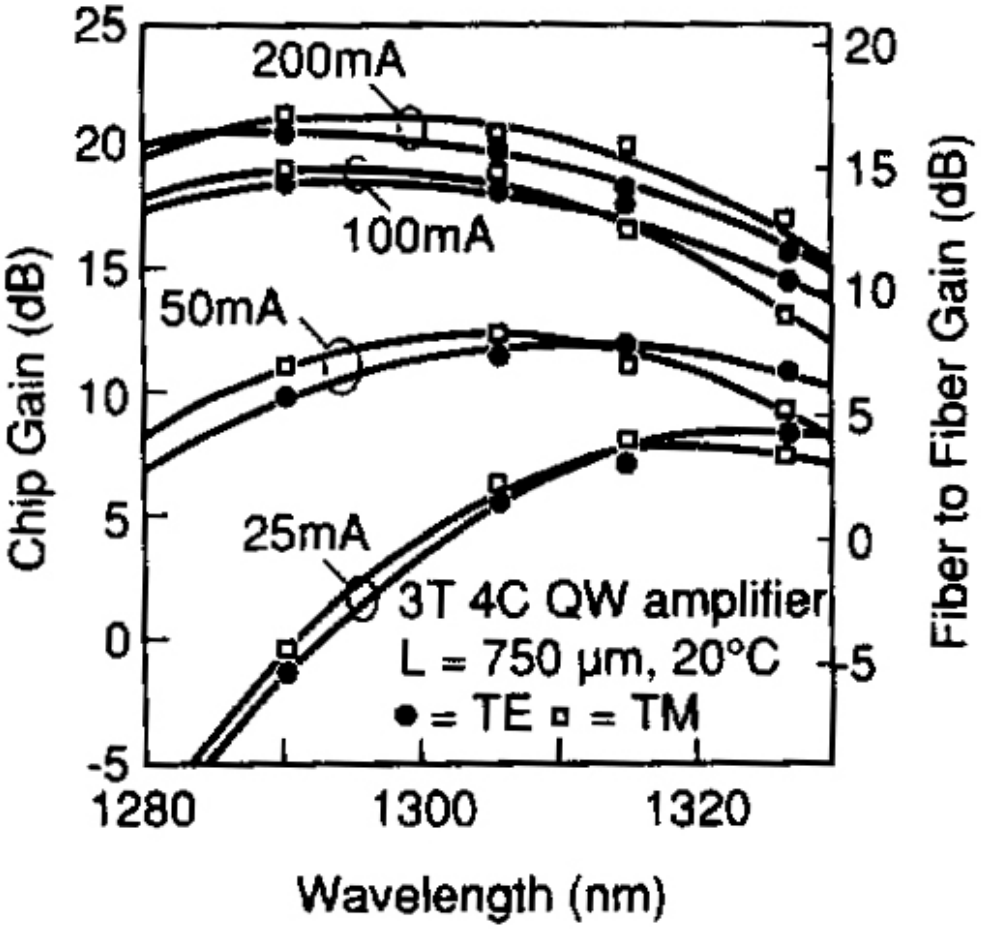




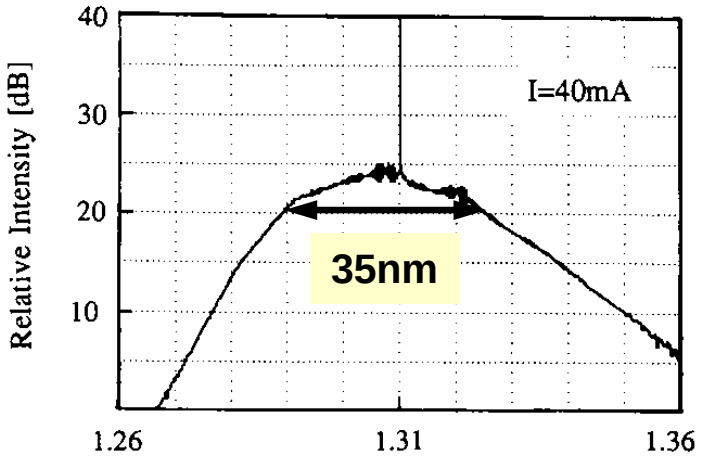


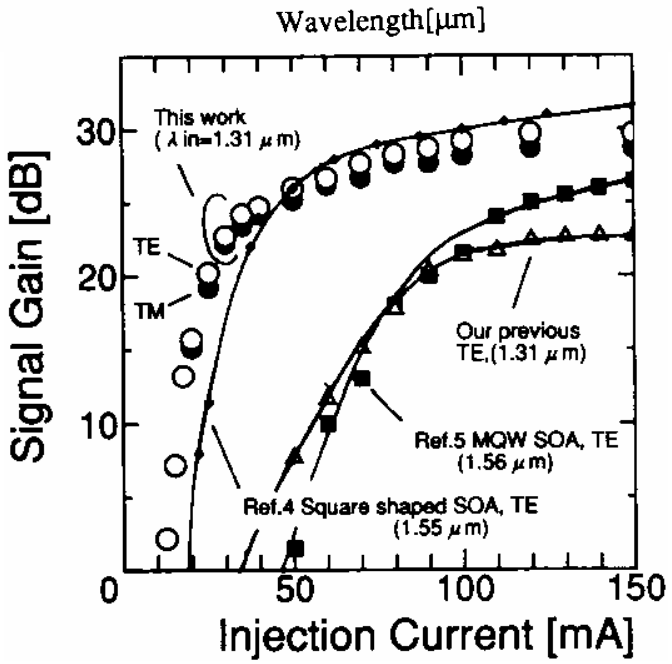


SOA at 1.3µm – Literature in the Public Domain



P. Thijs, J. Quantum Electronics, vol. 30, page 477, 1994





S. Kitamura, Photon. Tech. Lett., vol. 7, page 147, 1995

SOA's Issues and Mitigation

- SOA's have moderate gain
  - Usable gain (allowing for various margins) ~ 15dB
- Receiver applications need small polarization dependent gain (PDG); Historically SOA's have a reputation for very poor PDG
  - Modern fabrication techniques have improved PDG performance
  - PDG ~ 1dB
- SOA's have acceptable noise figure for intermediate reach applications
  - Without accounting for fiber coupling the NF ~ 4.5dB; With fiber coupling it could be 2dB higher
- SOA's have moderately wide gain spectrum
  - Typical 3dB spectral width is of the order of 30nm to 50nm
  - This is suitable for iWDM, but not CWDM applications
- SOA's are capable of multi-channel WDM operation
  - Actually SOA's prefer operating with multiple channels input at any one time to mitigate the effects of cross gain modulation

Key Considerations For 100GbE Monolithic Integration

- Range of active wavelengths (material bandgaps) required on a chip
  - 200-400 GHz WDM preferred to 20nm CWDM
- Wavelength Accuracy / Drift Requirements
  - 400GHz preferred to 200GHz
- Modulator Performance
  - 200GHz preferred over 400GHz
  - 400GHz preferred over 800GHz
- Designs for Longer Reach (i.e. 40km)
  - Likely requires a Rx SOA
  - Width of gain spectrum requires WDM (not CWDM) if using only one SOA (lowest cost / lowest power dissipation option)
- 400GHz Channel spacing is likely the preferred channel spacing for 100GbE solutions, **if** desiring to leverage/facilitate a range of monolithic integration solutions

Backup Slides

Cooled, Uncooled, Semi-Cooled, Always Hot …

- Some simple math

cWDM Options	Min	Max
Temperature Range of Operation (ºC)	-40	80
DFB Tuning with Temperature (GHz/ºC)	15	
Total Tuning Range of the DFB (GHz)	1800	
Total Tuning Range of the DFB (nm) at 1312nm	10.3	
Usable CWDM Filter Bandwidth (nm)	13	
Bandwith Allocated DFB/EMLManufacturing Tolerance (nm)	2.66	
Bandwith Allocated DFB/EML Manufacturing Tolerance (GHz))	464	

Although the channel spacing is 20nm for CWDM, for uncooled operation, the final manufacturing tolerance for EML is small.

iWDM Options			
Channel Spacing (GHz)	200	400	800
Bandwidth Allocated to Temperature Variation (%)	50%	50%	50%
Bandwidth Allocated to Temperature Variation GHz)	100	200	400
Bandwith Allocated DFB/EML Manufacturing Tolerance (GHz))	100	200	400
DFB Tuning with Temperature (GHz/ºC)	15	15	15
Total Temperature Range for Stabilization (ºC)	6.7	13.3	26.7

For iWDM, depending on how the performance over temperature is managed, the EML manufacturing tolerance is of the same order of magnitude as for the CWDM application.

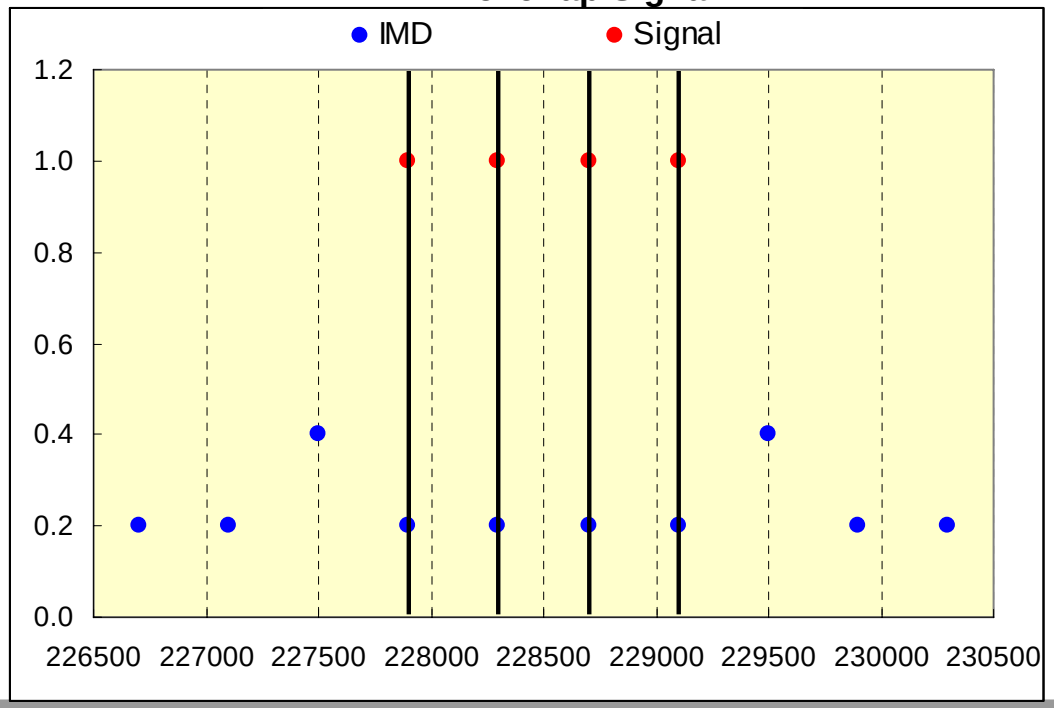
The EML/DML does not have to be cooled. If an EML can be designed to operate at 80ºC, then it can be designed to operate hot (with heating and not cooling) inside a ±10ºC range.

FWM a.k.a. IMD

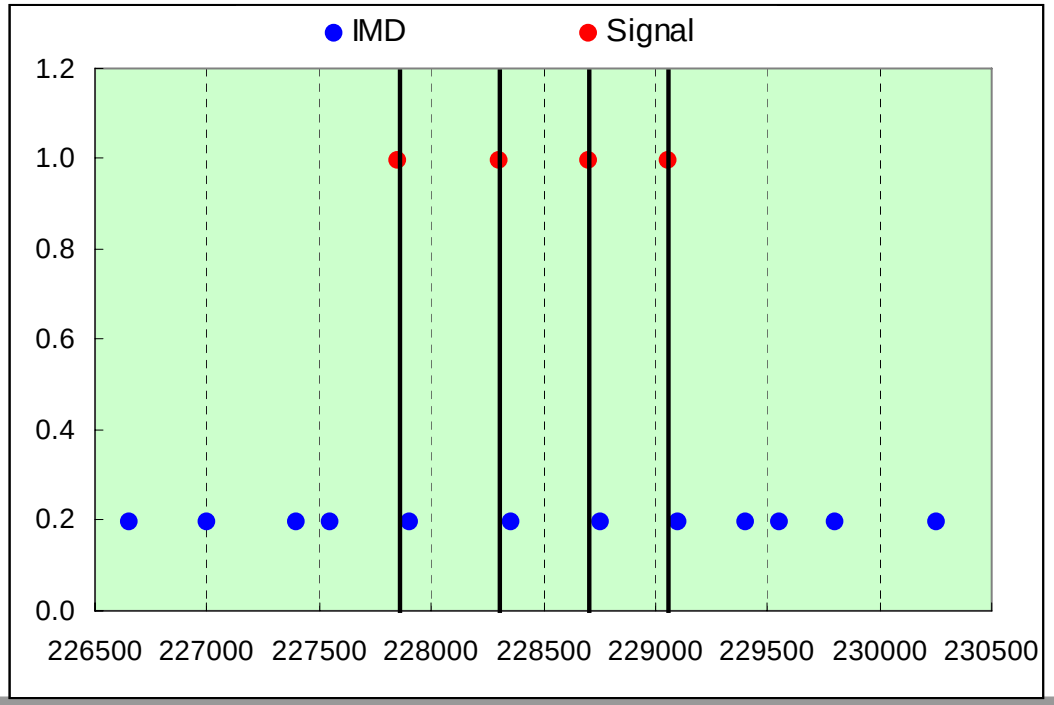
- **Four Wave Mixing or Intermodulation Distortion varies as P^3. Hence, it is very sensitive to input power. At the receiver, especially for 40km applications, the input optical power will generally be low. The impact of FWM will not be as severe.**

- **IMD is the most severe for channels that are equally spaced in frequency.**
- **Since the 100GbE may be implemented using just 4 wavelengths, it is relatively simple to use a slightly offset grid to eliminate the impact FWM.**

Equal Channel Spacing; 400GHz
IMD overlap Signal



Unequal Channel Spacing; 350GHz, 400GHz, 450GHz
Effect of IMD Eliminated



Photonic Integration – Demonstrable “Learning Curve”

Normalized increase in PIC output per wafer input