FEC applicability to 40 GbE and 100 GbE

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Outline

• Existing applications of Forward Error Correction in 802.3
  • VDSL (clause 62)
  • 1G EPON (clause 65)
  • 10G Backplane (clause 74)
  • 10G EPON (under development, clause 92)
• Possible needs for Forward Error Correction in 40GbE and 100 GbE
  • 40G Backplane
  • 40km SMF interface for 100 GbE
VDSL FEC - Clause 62

- FEC not specified directly in 802.3, but incorporated by reference to ANSI T1.424 VDSL standard
- Supports RS(144,128) and RS(240,224) coding
- Specific to voice-grade twisted pair environment - no apparent applicability to 40 GbE or 100 GbE
Clause 65 - 1G EPON FEC

- FEC is transmitted inband in a stretched IPG, reducing the total throughput of the interface
- Suitable for an environment with multiple subscribers, high split ratios, and where the number of subscribers can be reduced to allow optional FEC to be used without individual subscribers necessarily seeing a decrease in overall throughput
- RS(255,239) FEC per ITU-T G.975
Clause 65 - 1G EPON FEC

FEC applicability to 40 GbE and 100 GbE

Systematic FEC code leaves original frame unchanged while adding parity

Receiver can begin decode once 16 parity bytes are received for 1st 239 data bytes

Select T_FEC_E or T_FEC_O pattern depending on running disparity

Note: shorted last block “padded” to still produce 16 parity bytes

/s/ from one to 5 bytes for high BER environment

/t/ from one to 6 bytes for high BER environment

5 FEC applicability to 40 GbE and 100 GbE
Clause 74 - Backplane FEC

- Uses shortened cyclic code (2112, 2080) by shortening cyclic code (42987, 42955)
- Can correct error bursts up to 11 bits
- Well suited to error bursts in typical backplane channel resulting from error propagation in the receive equalizer
- Framing algorithm
  - Test candidate block start position
  - Descramble block and check for good FEC
  - No match, shift candidate block start by one bit position and try again
  - 4 consecutive blocks good FEC establishes framing; 8 consecutive blocks without good FEC loses framing and start over; from in-frame
  - While this is “brute force”, framing takes <5 Mbit on a 10 Gbit/s stream, <0.5ms
Clause 74 - Backplane FEC

Steal redundant SYNC bits from 32 66-bit blocks to create space for parity bits

Table 74-1 FEC Block Format

<table>
<thead>
<tr>
<th>T₀</th>
<th>64-bit payload Word 0</th>
<th>T₁</th>
<th>64-bit payload Word 1</th>
<th>T₂</th>
<th>64-bit payload Word 2</th>
<th>T₃</th>
<th>64-bit payload Word 3</th>
</tr>
</thead>
<tbody>
<tr>
<td>T₄</td>
<td>64-bit payload Word 4</td>
<td>T₅</td>
<td>64-bit payload Word 5</td>
<td>T₆</td>
<td>64-bit payload Word 6</td>
<td>T₇</td>
<td>64-bit payload Word 7</td>
</tr>
<tr>
<td>T₈</td>
<td>64-bit payload Word 8</td>
<td>T₉</td>
<td>64-bit payload Word 9</td>
<td>T₁₀</td>
<td>64-bit payload Word 10</td>
<td>T₁₁</td>
<td>64-bit payload Word 11</td>
</tr>
<tr>
<td>T₁₂</td>
<td>64-bit payload Word 12</td>
<td>T₁₃</td>
<td>64-bit payload Word 13</td>
<td>T₁₄</td>
<td>64-bit payload Word 14</td>
<td>T₁₅</td>
<td>64-bit payload Word 15</td>
</tr>
<tr>
<td>T₁₆</td>
<td>64-bit payload Word 16</td>
<td>T₁₇</td>
<td>64-bit payload Word 17</td>
<td>T₁₈</td>
<td>64-bit payload Word 18</td>
<td>T₁₉</td>
<td>64-bit payload Word 19</td>
</tr>
<tr>
<td>T₂₀</td>
<td>64-bit payload Word 20</td>
<td>T₂₁</td>
<td>64-bit payload Word 21</td>
<td>T₂₂</td>
<td>64-bit payload Word 22</td>
<td>T₂₃</td>
<td>64-bit payload Word 23</td>
</tr>
<tr>
<td>T₂₄</td>
<td>64-bit payload Word 24</td>
<td>T₂₅</td>
<td>64-bit payload Word 25</td>
<td>T₂₆</td>
<td>64-bit payload Word 26</td>
<td>T₂₇</td>
<td>64-bit payload Word 27</td>
</tr>
<tr>
<td>T₂₈</td>
<td>64-bit payload Word 28</td>
<td>T₂₉</td>
<td>64-bit payload Word 29</td>
<td>T₃₀</td>
<td>64-bit payload Word 30</td>
<td>T₃₁</td>
<td>64-bit payload Word 31</td>
</tr>
</tbody>
</table>

32 parity bits

$T_i=0 \leftrightarrow \text{Sync}=10 \quad T_i=1 \leftrightarrow \text{Sync}=01$

Additional scrambler to restore DC balance after removing one of the SYNC bits from each 66B block
### Clause 92 - 10G EPON FEC - under development

Key attributes of solution chosen, but not specific solution

<table>
<thead>
<tr>
<th>Motion</th>
<th>Text</th>
</tr>
</thead>
<tbody>
<tr>
<td>Orlando 3</td>
<td>10G EPON shall accommodate FEC's parity bandwidth by <strong>reducing</strong> the MAC's effective data rate (<strong>sub-rating</strong>).</td>
</tr>
<tr>
<td>Orlando 4</td>
<td>To accept the scheme outlined in slides 3-7 in <a href="#">3av_0703_mandin_2.pdf</a> as the baseline scheme for upstream FEC framing and synchronization.</td>
</tr>
<tr>
<td>Orlando 5</td>
<td>To accept as a baseline scheme the FEC codeword structure depicted in the illustration on slide 5 in <a href="#">3av_0703_mandin_2.pdf</a> for the downstream (so that the FEC codeword structures on the upstream and downstream are identical).</td>
</tr>
<tr>
<td>Geneva 6</td>
<td>The FEC algorithm shall be accept as its input Nx65bit payloads (the second bit of the sync header plus 64 bits of data) pre-pended with padding consisting of zeros to bring the input codeword to the required size; notwithstanding, both bits of the sync header shall be transmitted, while the padding shall not be transmitted, as illustrated in <a href="#">3av_0705_effenberger_4.pdf</a>.</td>
</tr>
<tr>
<td>Geneva 7</td>
<td>To accept as a baseline for FEC framing the presentations <a href="#">0701_effenberger_1.pdf</a>, <a href="#">0703_kramer_1.pdf</a> and <a href="#">0705_lynskey_1.pdf</a>.</td>
</tr>
</tbody>
</table>
Clause 92 - 10G EPON FEC - Possible Example

• FEC is computed on a 66B codeword basis
• M blocks of parity are added per N blocks of data
• FEC will add 7-15% depending on the code chosen

Example using RS(255,239)

Data is “normal” 66B blocks with SYNC=01 or 10

Pad with 8 bytes of zero to compute FEC over 239 bytes

16 parity bytes coded as two 66B blocks, SYNC=00 or 11
40 GbE and 100 GbE - Where might we need FEC?

- **40 GbE backplane**
  - Since 10G Base-KR needed FEC, 40 GbE backplane will likely require it
  - If 40 GbE backplane ends up looking like 4 lanes of 10G Base-KR at the
    PCS/physical layer, clause 74 FEC can likely be applied on a per-lane basis
    with little or no change

- **40 GbE or 100 GbE over metro or long-haul DWDM systems**
  - OTN Wrapper provides FEC - no need for it in Ethernet
  - RS(255,239) for cross-vendor interoperability
  - Vendor specific “Super-FEC” (many described in ITU-T G.975.1) for long-
    haul DWDM systems

- **100 GbE native 40km interface**
  - Not known if required
Possible FEC for 100 GbE native 40km interface, if needed

- Would EPON sub-rate FEC be acceptable? Probably not:
  - EPON is inherently used in a multi-subscriber environment where no individual subscriber gets the full bandwidth capability of the interface
  - End users who are dissatisfied with LAG because of bandwidth inefficiency with small numbers of large flows will likely not accept bandwidth reduction based on reach.

- IF FEC is required for 100 GbE 40km, it would most likely need to be super-rate (increase the lane rate to accommodate the parity) rather than sub-rate

<table>
<thead>
<tr>
<th>Example: 40km 4x25G DWDM interface using CTBI/virtual lane approach and RS(255,239)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Nominal lane rate without FEC, lane markers inband</td>
</tr>
<tr>
<td>Nominal lane rate without FEC, lane markers out of band</td>
</tr>
<tr>
<td>Nominal lane rate with RS(255,239) FEC, add 2 blocks to each 28, lane markers inband</td>
</tr>
<tr>
<td>Nominal lane rate with RS(255,239) FEC, add 2 blocks to each 28, lane markers out of band</td>
</tr>
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Possible format for 100 GbE 40km FEC format, if needed

- FEC is computed per physical lane on a 66B codeword basis
- M blocks of parity are added per N blocks of data, increasing the lane rate
- FEC will add 7-15% depending on the code chosen

Example using RS(255,239)

Note: If this technique were to be applied to 40 GbE, the format of the parity blocks is not transcodable to 512B/513B. However, the LAN FEC would be decoded before the adaptation into OTN (the LAN signal WITH added FEC wouldn’t fit standard ODU3 anyway)
Conclusions

• Assuming that 40 GbE backplane looks like four lanes of 10G Base-KR, clause 74 FEC can likely be reused
• Ethernet FEC is not needed for metro and long-haul DWDM applications, as OTN takes care of these cases
• IF FEC is required the 40km 100GbE interface, it likely needs to be a super-rate solution (increasing the lane bit-rate to add parity). The technique of adding $M$ parity blocks to $N$ 66B data blocks under consideration in 802.3av could likely be applied