Proposal of PMD architectures for HSSG

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Outline

- Proposal of Parallel PMDs
  - Transmission Rate
  - Transmission Reach
- Future Challenges
  - Skew compensation
  - Electrical interface
  - Error correction
  - EDC
Market

- Improvements
  1. FTTH upgrade
     - Increasing bandwidth
  2. Content
     - Increasing bandwidth requirements
       - HDTV
  3. Backbone Network
     - Metro area: Internet Service Providers
       - Today 10 – 40 Gbps, Next 100 Gbps
     - Data Center
Requirements

- Wider Bandwidth: ~ 100 Gbps
- Longer Reach: 100 m ~ 80 km
  - APL will be feasible for long-haul transmission
- Low Cost:
  - Small number of optical components
  - Compact CMOS-ICs
- Low Power Consumption
- Low Latency
Brainstorming possible PMD architectures

- **10 ch architectures** (technically easy)
  - -> **4ch architectures** (cost effective)

EA-DFB: DFB integrated with Electro-absorption modulator
Possible PMD architectures (25 Gbps x 4 ch)

<table>
<thead>
<tr>
<th>#</th>
<th>Name</th>
<th>Method (pitch)</th>
<th>LD</th>
<th>PD</th>
<th>Wave-length</th>
<th>Fiber</th>
<th>Reach</th>
</tr>
</thead>
<tbody>
<tr>
<td>1-1</td>
<td>LC4</td>
<td>CWDM (24.5 nm)</td>
<td>Un-cooled EA-DFB</td>
<td>PIN</td>
<td>13xx</td>
<td>SMF</td>
<td>10 km</td>
</tr>
<tr>
<td>1-2</td>
<td></td>
<td>DWDM (8 nm)</td>
<td>Cooled DFB</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>EC4</td>
<td>CWDM 24.5 nm</td>
<td>Un-cooled EA-DFB</td>
<td>APD</td>
<td>13xx</td>
<td>SMF</td>
<td>40 km</td>
</tr>
<tr>
<td>3</td>
<td>SC4</td>
<td>Ribbon</td>
<td>DFB</td>
<td>PIN</td>
<td>1310</td>
<td>SMF Ribbon</td>
<td>300 m</td>
</tr>
</tbody>
</table>

- CWDM pitch (24 nm): equal to LX4
- DFB-LD (low-cost) requires 8-nm DWDM pitch for 10-km transmission
Estimation: 25 Gbps x 4 ch

EA-DFB Dispersion Tolerance: 1600 nm/ps, DFB: 170 nm/ps
Minimum Optical Receiver Power @ 25 Gbps; PIN: -14 dBm, APD: -23 dBm
### Possible PMD architectures (10 Gbps x 10 ch)

<table>
<thead>
<tr>
<th>#</th>
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<th>PD</th>
<th>CH</th>
<th>Wave-length</th>
<th>Fiber</th>
<th>Reach</th>
</tr>
</thead>
<tbody>
<tr>
<td>4-1</td>
<td>ZC10</td>
<td>DWDM (0.8 nm or 1.6 nm)</td>
<td>Cool EA-DFB</td>
<td>PIN</td>
<td>10</td>
<td>15xx</td>
<td>SMF</td>
<td>40 km</td>
</tr>
<tr>
<td>4-2</td>
<td></td>
<td></td>
<td></td>
<td>APD</td>
<td>10</td>
<td>15xx</td>
<td>SMF</td>
<td>80 km</td>
</tr>
<tr>
<td>5</td>
<td>SC10</td>
<td>Ribbon</td>
<td>VCSEL</td>
<td>PIN</td>
<td>10</td>
<td>850 (13xx)</td>
<td>MMF Ribbon</td>
<td>300 m</td>
</tr>
</tbody>
</table>

- DWDM pitch (0.8 nm/1.6 nm): equal to ITU-grid
  - Wide pitch: prefer to monolithic integrated LD array
Estimation: DWDM 10 Gbps x 10 ch

- Dispersion Limit; lambda pitch: 0.8 nm
- Dispersion Limit; lambda pitch: 1.6 nm
- Loss limit (using AWG and PIN)
- Loss limit (using AWG and APD)

Channel bit rate (Gbps/ch) vs. distance (km)

- ZC10 #4-2
- ZC10 #4-1

Estimation: DWDM 10 Gbps x 10 ch
Future Challenges

- Skew Compensation in PCS
  - Between parallel links
- Electrical Interface
  - 25 Gbps x 4 ch (XENPAK) (or 12.5 Gbps x 8 ch ?)
- Error Correction
  - TBD
- EDC
  - TEB
Skew compensation

- Max. Skew
  - CWDM (4 wavelengths: 13xx nm): +/- 2 ns(10 km), +/- 8 ns(40 km)
  - DWDM (10 wavelengths: 15xx nm): +/- 7 ns(40 km), +/- 14 ns(80 km)
  - Short reach: 10 ribbon fiber- +/- 10 ns(100 m) ~ +/- 30 ns(300 m)

Example: 10 Gbps x 10 channels
How to detect skew

- **TX side**
  64B66B based special data pattern into IFG is sequentially output in all lanes at the same time.

- **RX side**
  Skew between the lanes is detected based on the difference in timing of received signal.

In this example: all signals are IDLE
Summary

- Parallel link
  - 25 Gbps x 4 ch (CWDM, DWDM and Ribbon)
  - 10 Gbps x 10 ch (DWDM and Ribbon)
- Reach Target (EA-DFB/DFB, PIN/APD)
  - 100 m, 300 m, 10 km, 40 km, 80 km
- Technical Challenges
  - Skew compensation
  - Electrical interface
  - Error correction
  - EDC