Objectives for HSSG

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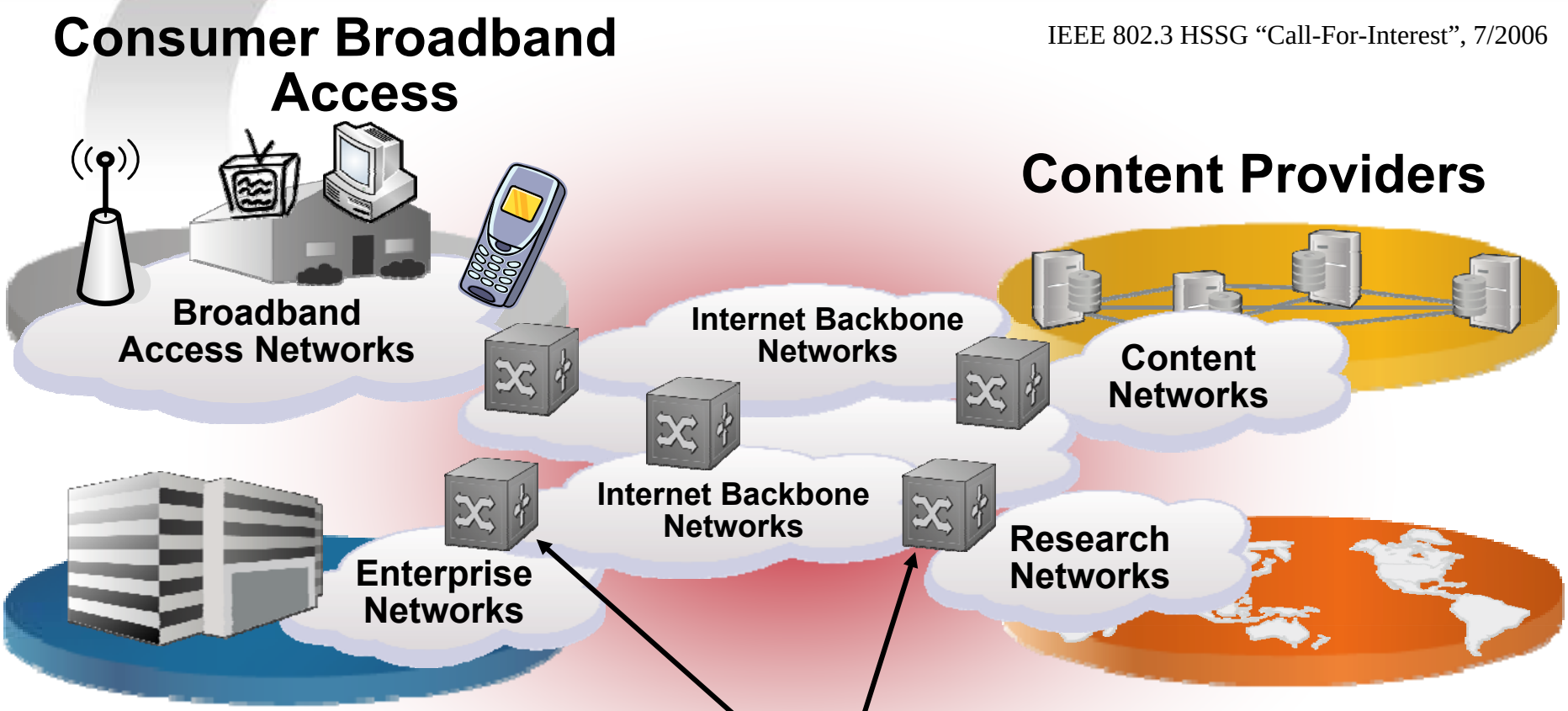
Agenda

- Propose objectives for:
  - MAC Data Rate
  - Reach Objectives
  - Standardize yGMII Interface
  - BER

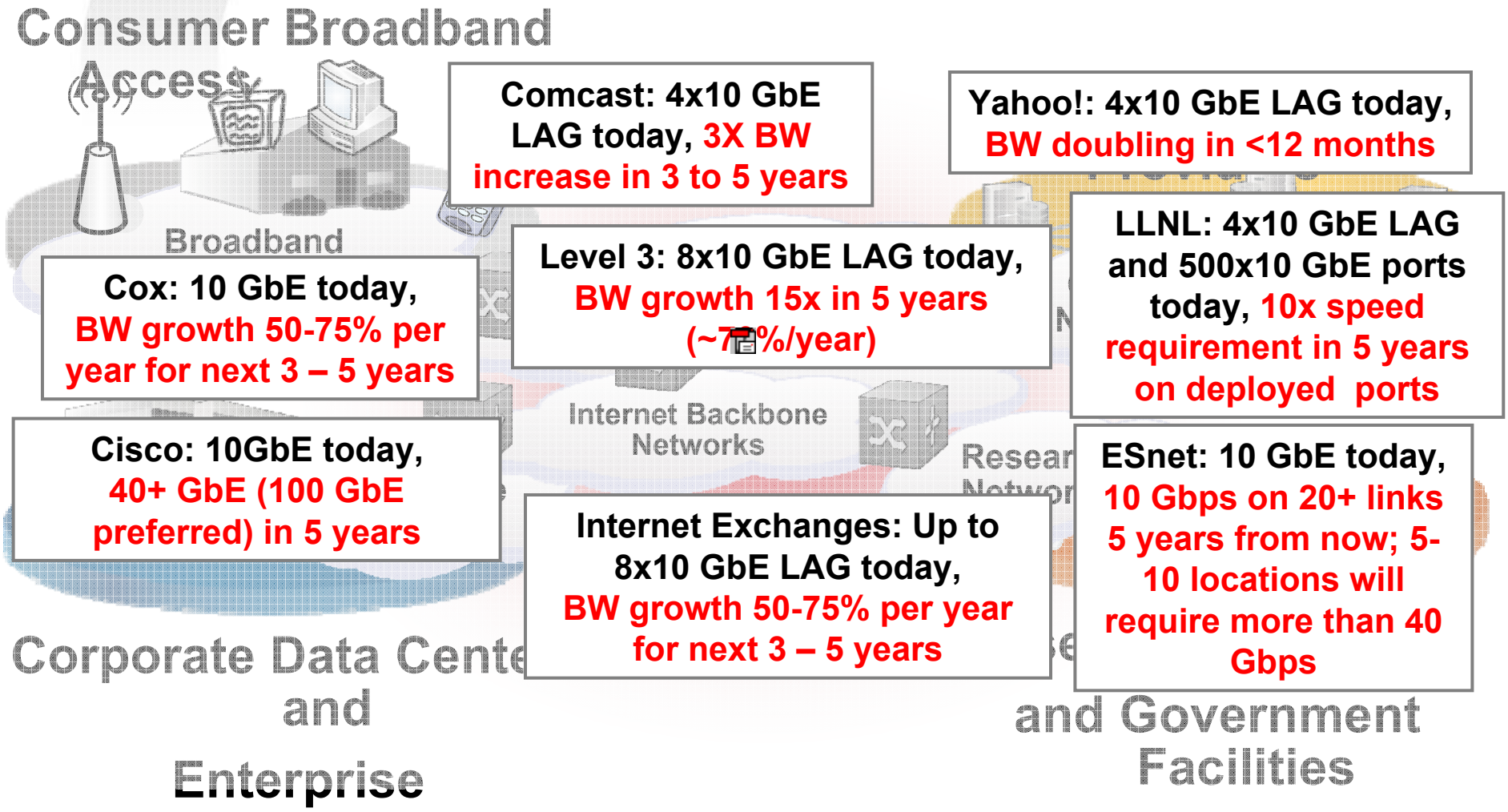
The Ethernet Ecosystem

IEEE 802.3 HSSG "Call-For-Interest", 7/2006



Bandwidth and Growth Projections

IEEE 802.3 HSSG "Call-For-Interest", 7/2006



Comcast: 4x10 GbE LAG today, 3X BW increase in 3 to 5 years

Yahoo!: 4x10 GbE LAG today, BW doubling in <12 months

Cox: 10 GbE today, BW growth 50-75% per year for next 3 – 5 years

Level 3: 8x10 GbE LAG today, BW growth 15x in 5 years (~7[illegible]%/year)

LLNL: 4x10 GbE LAG and 500x10 GbE ports today, 10x speed requirement in 5 years on deployed ports

Cisco: 10GbE today, 40+ GbE (100 GbE preferred) in 5 years

Internet Exchanges: Up to 8x10 GbE LAG today, BW growth 50-75% per year for next 3 – 5 years

ESnet: 10 GbE today, 10 Gbps on 20+ links 5 years from now; 5-10 locations will require more than 40 Gbps

MAC Data Rate Objective

- MAC Data Rate Objective – 100 Gb/s
  - 40 Gb/s insufficient
    - Traffic is surpassing this today
    - Can be achieved with 4 x 10 GbE LAG
  - Scaleable Data Rate not desirable
    - It's Ethernet
      - Cheap
      - Simple
      - Interoperable
    - Lane bonding approach acceptable to achieve 100 Gb/s
- Objective – should support Clause 43 LAG

Consideration of Reach Objectives

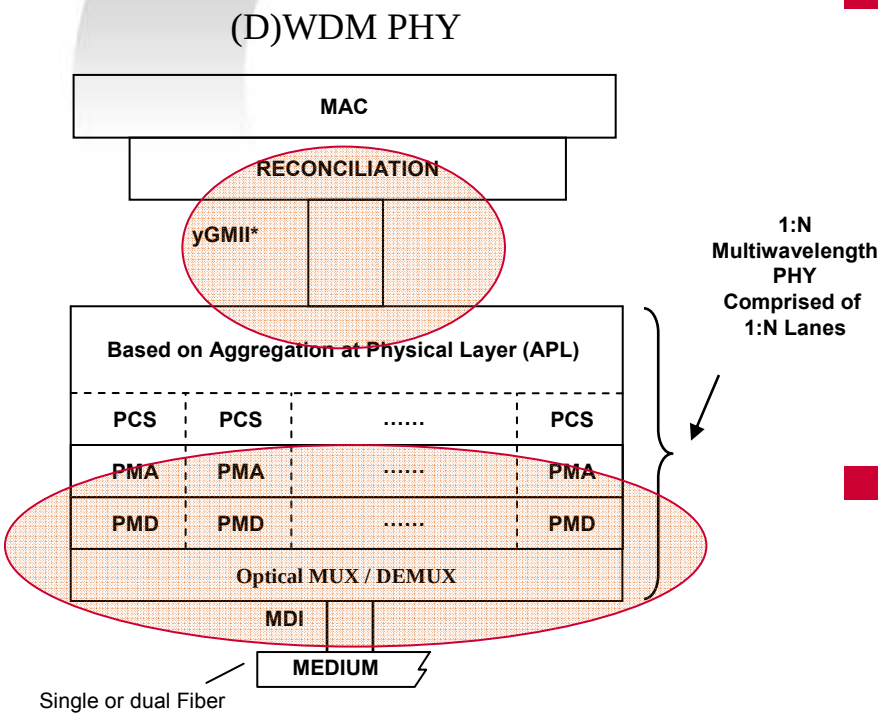
- Summary of 10GbE today

Fiber	10GBASE-SR / W	850 nm	Serial	300 / 33 m	50 um / 62.5 um MMF
	10GBASE-LRM	1310 nm	Serial	220 m	50 um / 62.5 um MMF
	10GBASE-LX4	1310 nm	WDM	300 m	50 um / 62.5 um MMF
				10 km	Single Mode Fiber
	10GBASE-LR / W	1310 nm	Serial	10 km	Single Mode Fiber
	10GBASE-ER / W	1550 nm	Serial	40 km	Single Mode Fiber
	10GBASE-ZR / W*	1550 nm	Serial	80 km	Single Mode Fiber
Copper	10GBASE-CX4		4 Lanes	15 m	Twinaxial
	10GBASE-T		4 Pairs	100 m	UTP (CAT6A)
Backplane	10GBASE-KX4		4 Lanes	1 m	Improved FR-4
	10GBASE-KR		Serial	1 m	Improved FR-4

* - Not specified by IEEE Std. 802.3

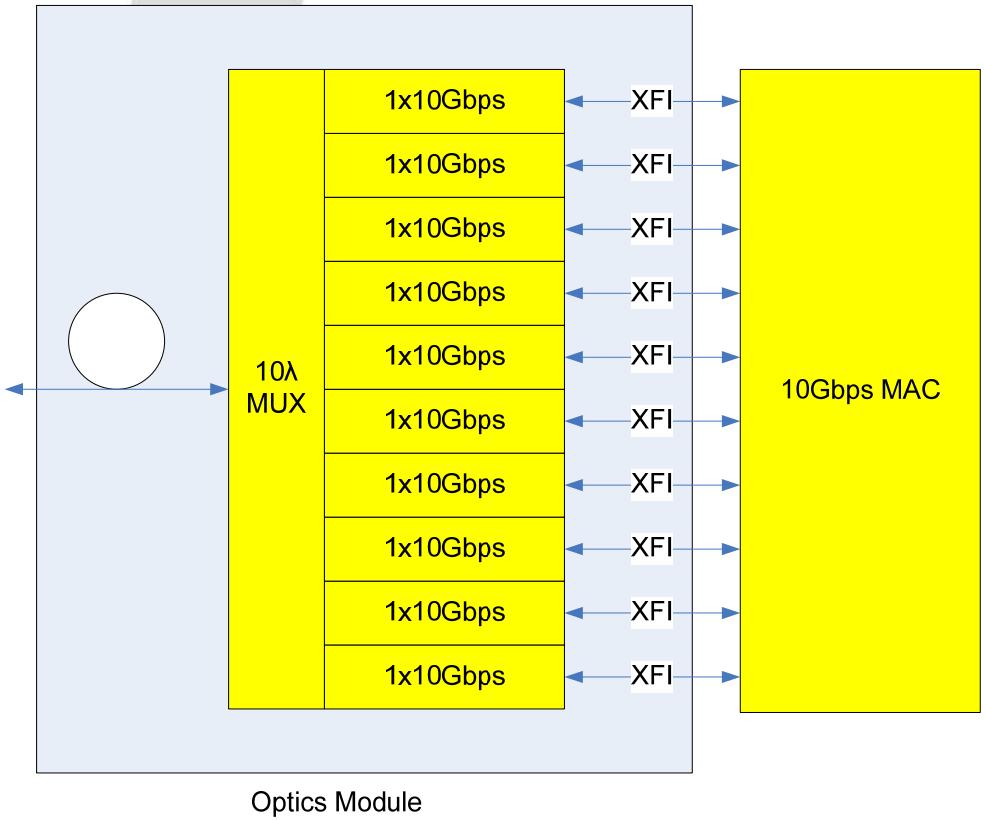
- Suggested Reach Objectives – 300 m / 10 to 40 km

Architecture Considerations



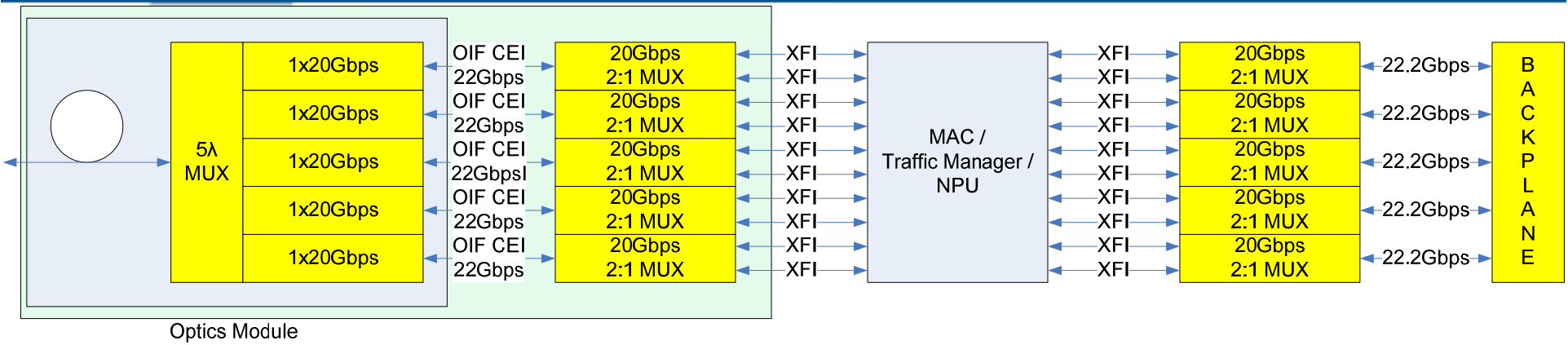
- yGMII Interface
  - Objective should be added to standardize interface
  - Needs to make sense in relation to PMD
  - No shims wanted
- yGMII / PMD
  - Need an architecture that allows pin count reduction in future
  - Example
    - Gen 1: 10 Gb/s per lane / λ
    - Gen 2: 20 Gb/s per lane / λ
    - Gen 3: 100 Gb/s per λ

Front-End Architecture Example: 100Gbps 10λx10 Interface



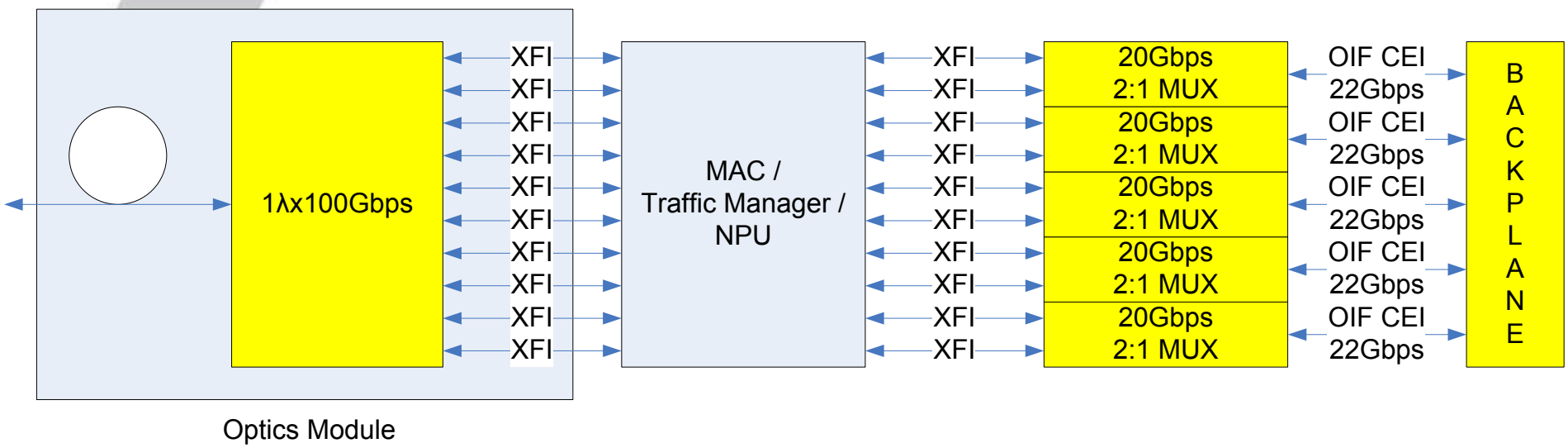
- Great WAN Interface
- Could be ….
  - Coiled out of the module
  - LC or SC
  - Larger then 300pin MSA non-pluggable
- Best density: one per blade … Maybe two.

Front-End Architecture Example: 100Gbps 5λx20 Interface



- Efficient LAN Interface
  - Would be dense enough to place four per blade
- 22.2Gbps CEI SERDES could be used front end and back end.
- Module could be XENPAK size with Launch cable coiled within the blade or possible direct fiber connectors for short reach
- Power efficient / Space efficient / Easiest to route.
- ASIC Technology in complex environments such as the NPU will limit SERDES to about 10Gbps per channel.

Front-End Architecture Example: 100Gbps 1λx100 Interface



- Probably 2013 … May not be cost effective for either LAN or WAN applications until about that time frame
- Would be dense enough to place four per blade
- XFI interface could be replaced with five lanes of 22.2Gbps CEI

BER … Thoughts

- Channel BER
  - Customers want to see a frame loss of zero
  - Systems architects want to see a frame loss of zero
  - Zero error is difficult to test and verify … none of us will live that long
- BER should be tested to 10E-12
  - Component cost is a real issue
  - It can be tested and verified at the system design level
- Standardize extrapolation to 10E-15

Summary Slide

- MAC Data Rate should be 100 Gb/s
- Solution should support Clause 43 LAG
- Specify yGMII Interface
- Specify Lane / λ architecture that makes sense
- Test BER to 10^-12
- Standardize extrapolation of BER to 10^-15