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Consider Transceiver Interfaces for 100G and 40G Ethernet PCS/PMA

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YOUR PARTNER FOR SUCCESS

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Supporters

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- Ali Ghiasi; Broadcom
- Matt Traverso; Opnext
- Wenbin Jiang; JDSU
- John Dallesasse; Emcore
- David Li; Ligent
- Mike Dudek; JDSU
- Ken Jackson; Emcore

Motivation

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Provide PCS/PMA interfaces suitable for a wide variety of transceiver applications (PMD's)

- **Optics:**
  - Parallel fiber optics
  - Serial transceivers
  - WDM/CWDM transceivers
- **Copper:**
  - Cable (direct attach) jumpers
  - Backplanes (for 40G only)

10GbE Architecture Interfaces

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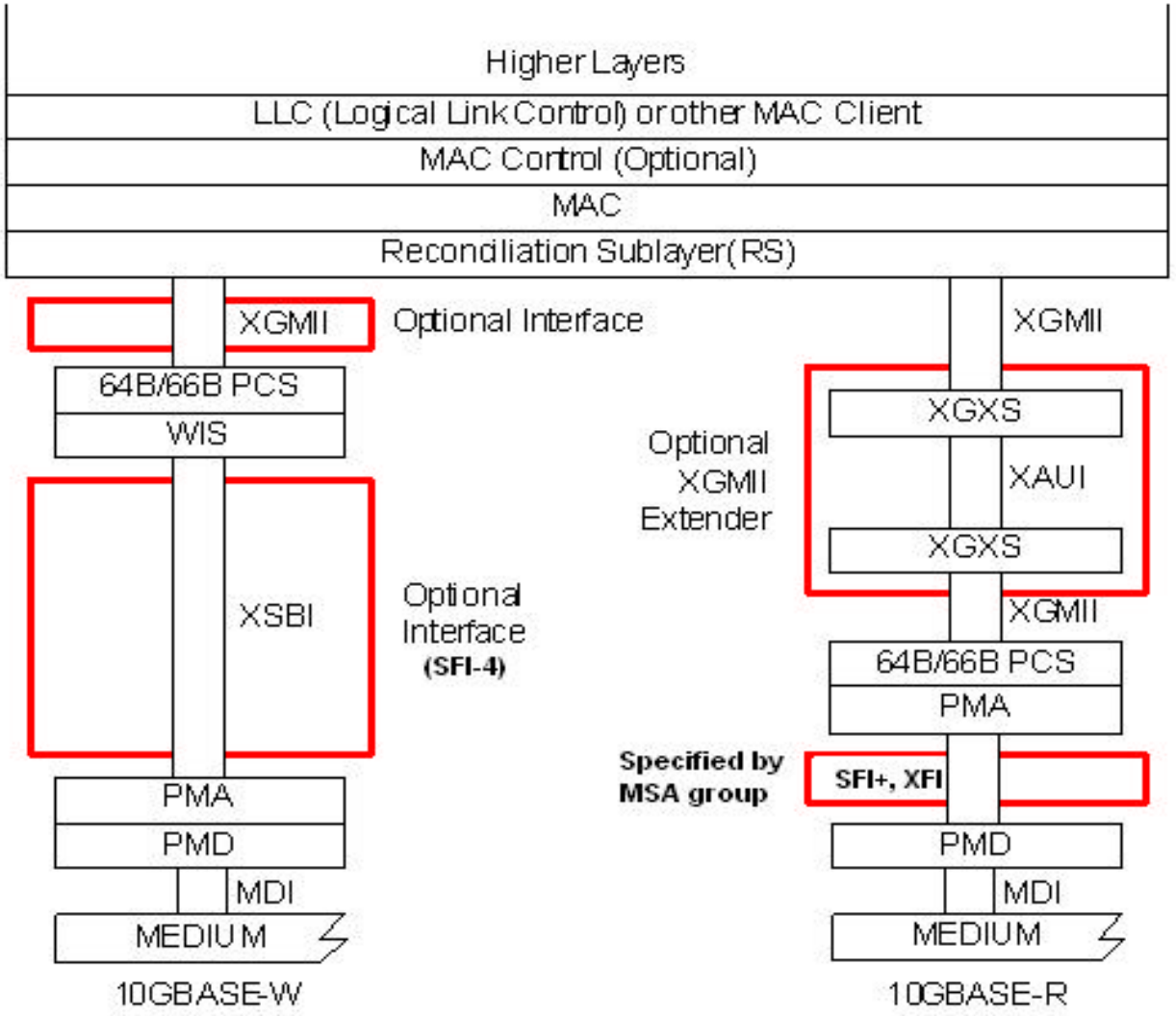
- Optical transceivers: Xenpak/X2, XFP, SFP+, 300-pin, QSFP, X40, …..



Review 100G Layered Interfaces

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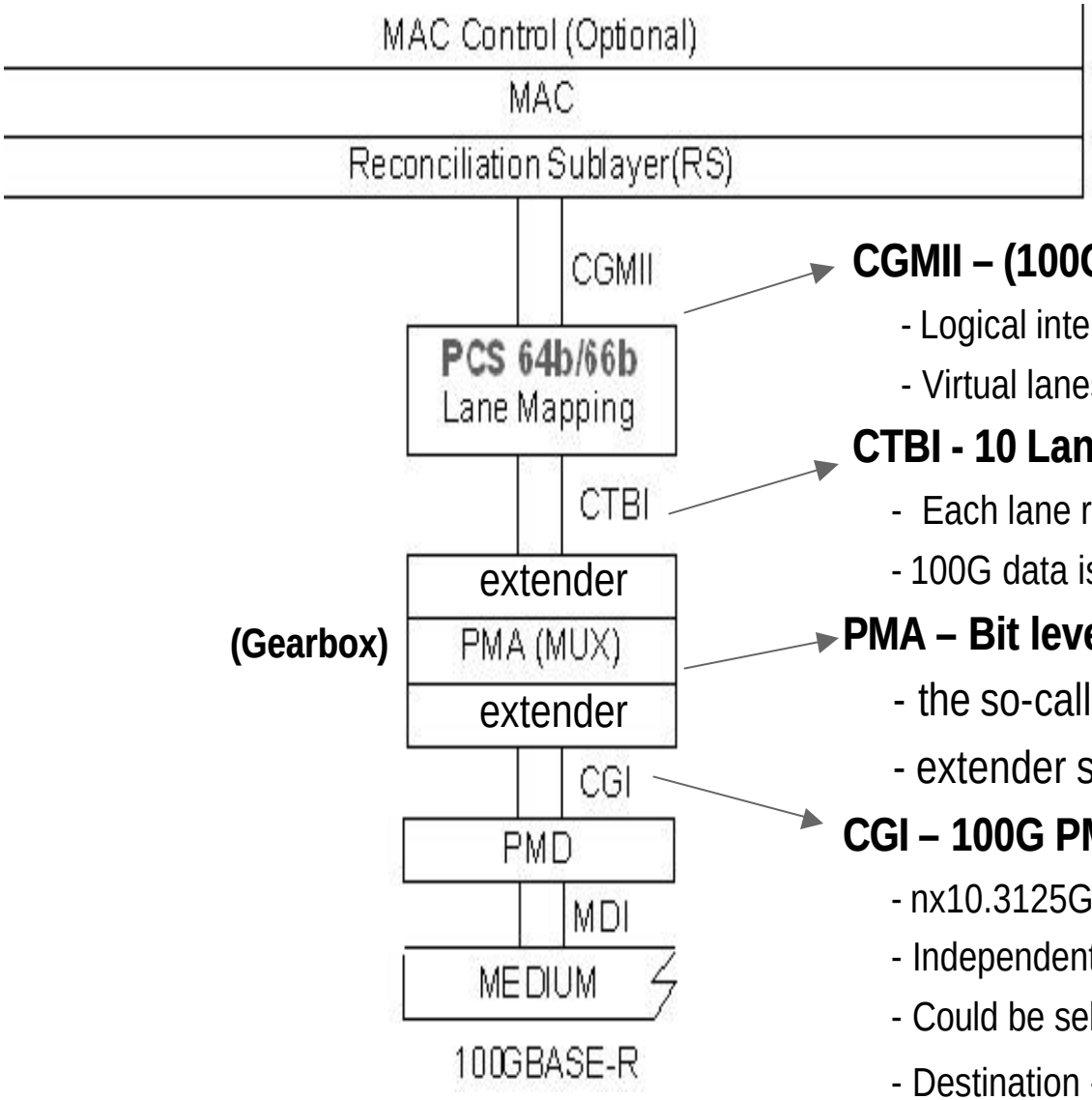

CGMII – (100G Media Independent Interface)

- Logical interface from or to the MAC
- Virtual lanes of 10G based on 64B/66B blocks

CTBI - 10 Lane MAC/PCS to PMA Interface

- Each lane runs at 10.3125G
- 100G data is inverse muxed across the CTBI lanes

PMA – Bit level MUX/DeMUXing

- the so-called "Gearbox"
- extender sublayers for 100G elec./optical

CGI – 100G PMA to PMD interface

- nx10.3125G (MMF or Cu), or 4x 25G (SMF) lanes
- Independent Tx/Rx paths
- Could be self-timed or non-timed interface.
- Destination - Deskew/sync

***Source:** Sub K., gustlin_01_0107.pdf*

PCS and PMA interfaces

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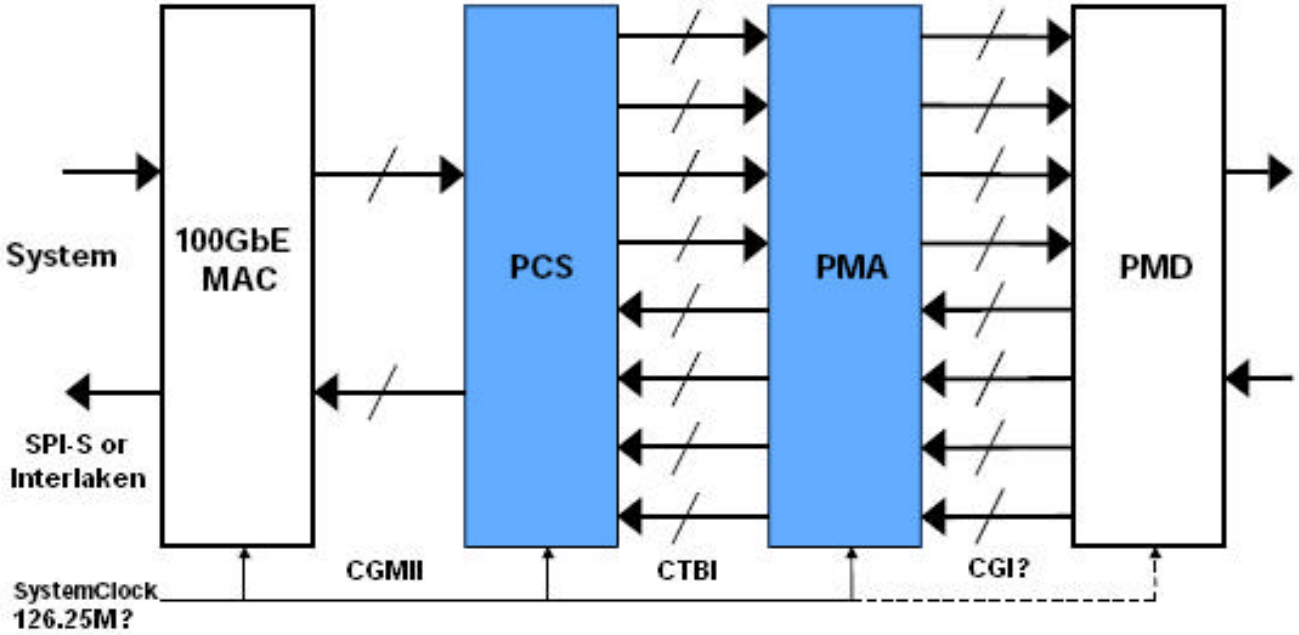

(100G and 40G implementation can be similar)

- **Generic PCS: provide coding for optical and electrical**
  - **Skew control: gustlin_01_0107.pdf**
- **PMA: High speed parallel serdes and bit-level muxing**
  - PMA could be silicon process different from PCS or PMD.
- **Critical questions:**
  - How many chips are considered necessary?
  - Possibly simpler (PMD only) optical modules?

Interface reach discussion

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Compare 10G interfaces:

- XAUI - 20” (50cm) over FR-4 (0 – 2 connectors)
- XGMII – Limited to ~7cm (per 46.1.5)
- 10GBASE-KR – 40” (100cm) over improved FR-4 plus 2 connectors
- CEI-11G-SR - 8” over improved FR-4 plus 1 connectors (CEI-25 is also proposing)
- XFI - 8” (20cm) Plus 1 connector
- SFI - 8” (20cm) Plus 1 connector

What will the 100G interfaces be?

- For CGI –
  - 8” over improved FR-4 plus 1 connector???
- For CTBI –
  - 8” over improved FR-4 plus 1 connector???

Summary - PMD Objectives

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- Physical Layer Signaling Specifications to be developed for:

	40G	100G
At least 1m backplane	√ **(4x -KR)**	
At least 10m cu cable	√ **(4x -T)**	√ **(10x -T)**
At least 100m OM3 MMF	√ **(4x array)**	√ **(10x array)**
At least 10km SMF		√ **(4x 25G EML)**
At least 40km SMF		√ **(4x 25G EML)**

Transceiver Options

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- Transponders having full PMA/PMD
  - Example: Xenpak/X2, 300-pin
  - Typically costly and high power dissipation
- Retimed serial transceivers
  - Example: XFP(-E), X40
  - power dissipation concern
- Non-retimed serial transceivers
  - Example: SFP+, QSFP, SNAP12
  - PMD only, tight jitter specs, require host equalization
- Parallel Optical Transceiver
  - Examples: QSFP, SNAP12
  - PMD only, low cost, but very short distance
- WDM/CWDM Transceiver
  - Example: LX4, X40

Some discussion in

aronson_01_0707.pdf;
ghiasi_01_0707.pdf

SFP+ Limiting vs. Linear

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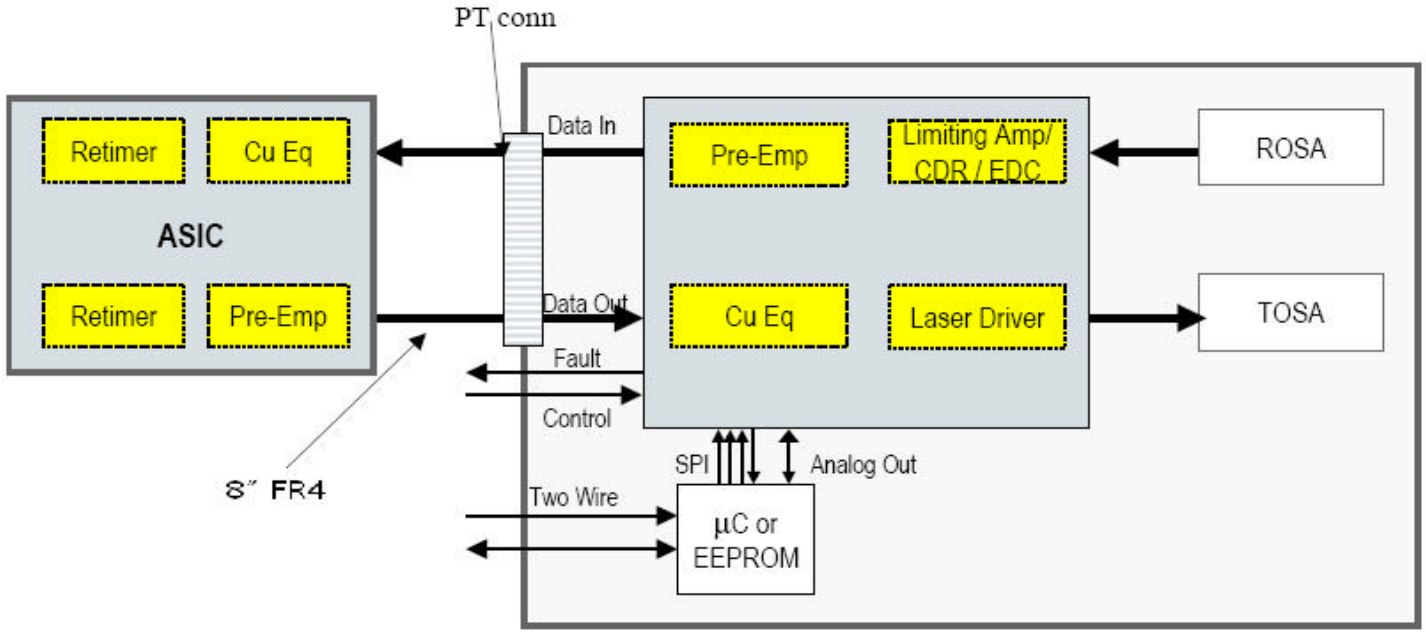
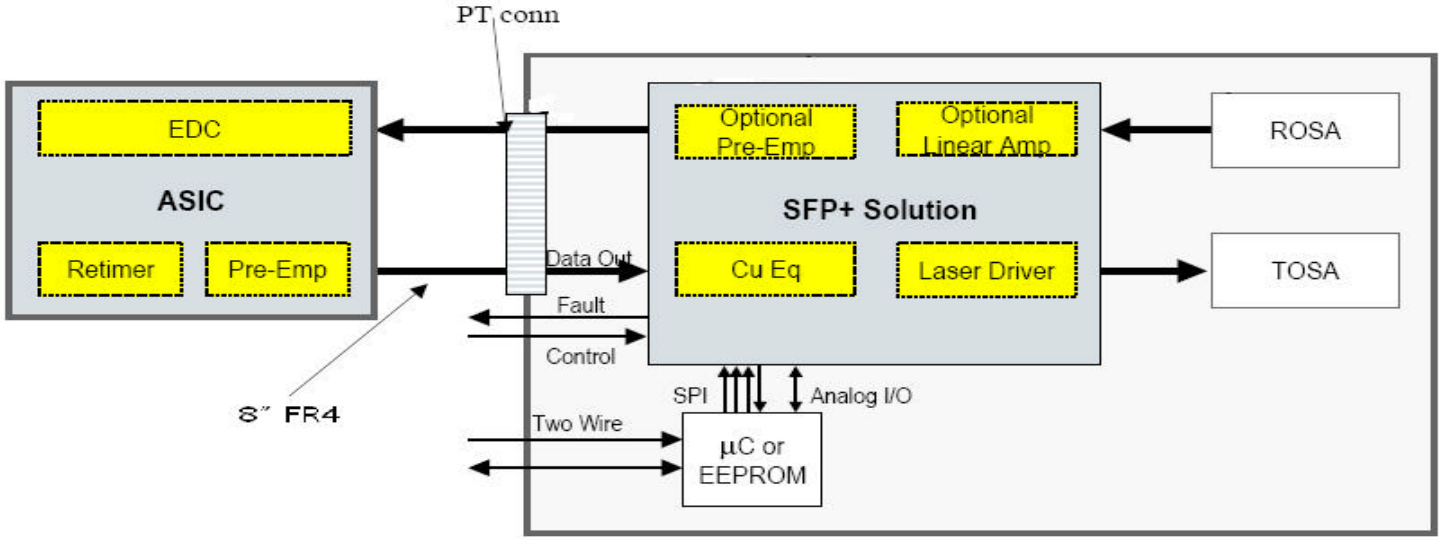
- Limiting



- Linear



SFP+ Limiting vs. Linear

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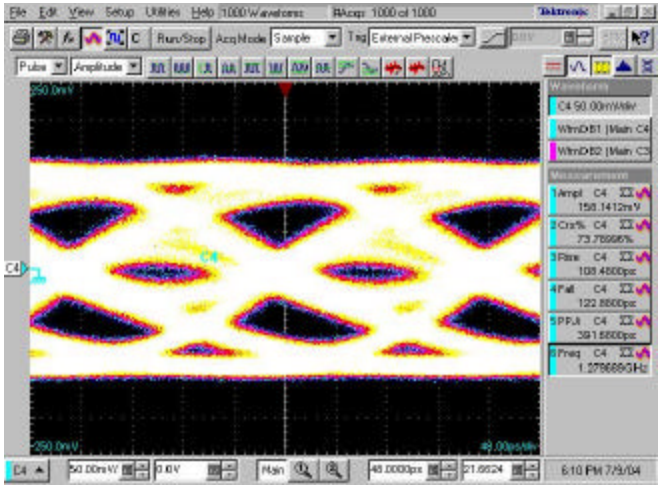
- EDC can use the signals from linear Rx to increase link lengths or provide margin by requiring less SNR than limiting Rx.
  - As standard feature now in 10G PHY, still some benefits when limiting.
  - For 100m OM3, EDC assumed(?) a much easier equalizer than LRM EDC.
  - Equalizers for 25G need further efforts (CEI-25G)
- Powerful EDC like for LRM open possibility to use low bandwidth/cost optics
  - Low-cost TOSA and ROSA exist for <4.25G in volume
  - EDC compensates the strong ISI distortion due to extra channel effects.
  - Such extra margin can offset penalties induced by EDC back-reflection noise, xtalks, jitter etc.
- Enhanced PCS with FEC coding
  - Currently employed in 10G-KR
  - FEC coding enable NECG of 2 - 2.5dB
  - RX operates well beyond 10^{-12} (typical 10^{-15})
  - Correct possible burst errors.
  - No change in line rates of 10.3125Gb/s

4G ROSA output Eye (running at 10.3G after 150m OM3 and 8" FR4 with 4G VCSEL)



What Matters?

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Still early-stage on discussing interface technical specs at 802.3ba.

- What will be the transceiver electrical interface?
  - How it looks like? Retimed or SFP+ type? Limiting or linear?
  - Could be in terms of transceivers or transponders?
  - Who will define this? By 802.3ba or outside MSA group?
- 10x10G and 4x10G first; then 4x25G?
  - Leverage 10G expertise with multi-lanes, again straightforward way to 40G/100G.
  - Reuse the existing 10G PMD/PHYs, electrical I/Os
- 4x25G PMA supported by SiGe TODAY, by CMOS tomorrow.
  - 4x25G is most acceptable for SMF PMD which is considered as low cost/power option.
- Use EDC for extra margin, enable low cost optics,
  - Compensate channel effects and reduce the effect of xtalk.
  - Linear or limiting?
- How about 10G-KR type coded FEC?
  - 10G-KR FEC provide ~2.5dB coding gain, without line rate increase.

Direction forward

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- We have lessons learned from 10GbE asking for limiting the number of PHY/PMD interfaces, and module form factors.
  - *How many is too many?*
- **Suggest to create a study (ad hoc) sub-group to define the optimal interface solution(s) for transceivers.**
  - Maximize the reuse of 10G chipsets and specs.
  - Minimize the number of new silicons to develop.
  - Probably need to revisit channel requirements