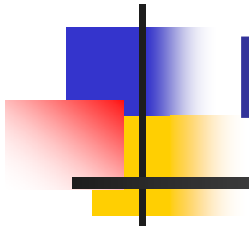

Implementation of Differential Precoder for DQPSK

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Introduction

- Single-wavelength transmission is important, and DQPSK can be achieved.
- From the viewpoint of technical feasibility, a differential precoder is one of the key issues
  - Serial-type precoder may be feasible for 40-Gbit/s transmission, but not for 100 Gbit/s.
- We tried to implement a parallel precoder for DQPSK using FPGA and ASIC.

DQPSK: Differential Quadrature Phase Shift Keying
FPGA: Field Programmable Gate Array
ASIC: Application Specific IC

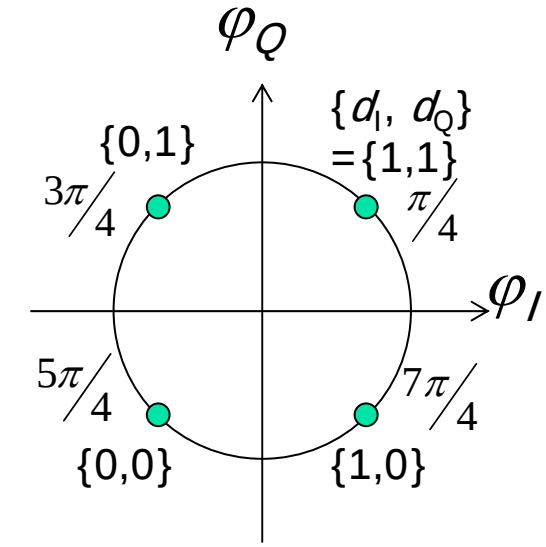
About Differential Precoder for DQPSK

- Differential precoder circuit calculates the difference in optical phase between symbols on the Tx.

$$\theta(n) = \phi(n) - \phi(n-1) \quad (\mathrm{mod}.2\pi)$$

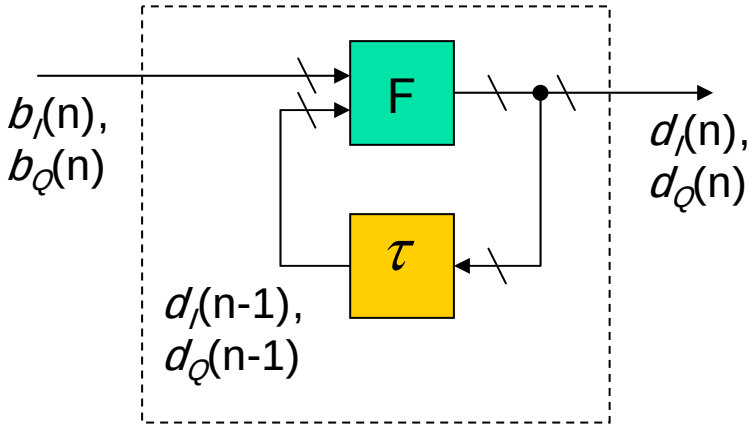
$$b_{I,Q}(n) = d_{I,Q}(n) - d_{I,Q}(n-1)$$

- Must operate serial precoder at 50 GHz to obtain 100 Gbit/s



DQPSK symbol allocation

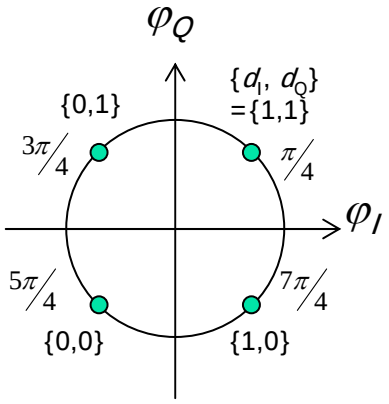
$$d_I(n) = b_I(n)\cdot b_Q(n)\cdot d_I(n-1) + \overline{b_I(n)}\cdot b_Q(n)\cdot \overline{d_Q(n-1)}$$
$$+ \overline{b_I(n)}\cdot \overline{b_Q(n)}\cdot \overline{d_I(n-1)} + b_I(n)\cdot \overline{b_Q(n)}\cdot d_Q(n-1)$$
$$dQ(n) = b_I(n)\cdot b_Q(n)\cdot d_Q(n-1) + \overline{b_I(n)}\cdot b_Q(n)\cdot d_I(n-1)$$
$$+ \overline{b_I(n)}\cdot \overline{b_Q(n)}\cdot \overline{d_Q(n-1)} + b_I(n)\cdot \overline{b_Q(n)}\cdot \overline{d_I(n-1)}$$



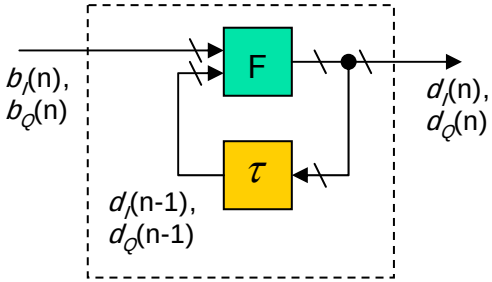
Serial precoder

Configuration of precoder

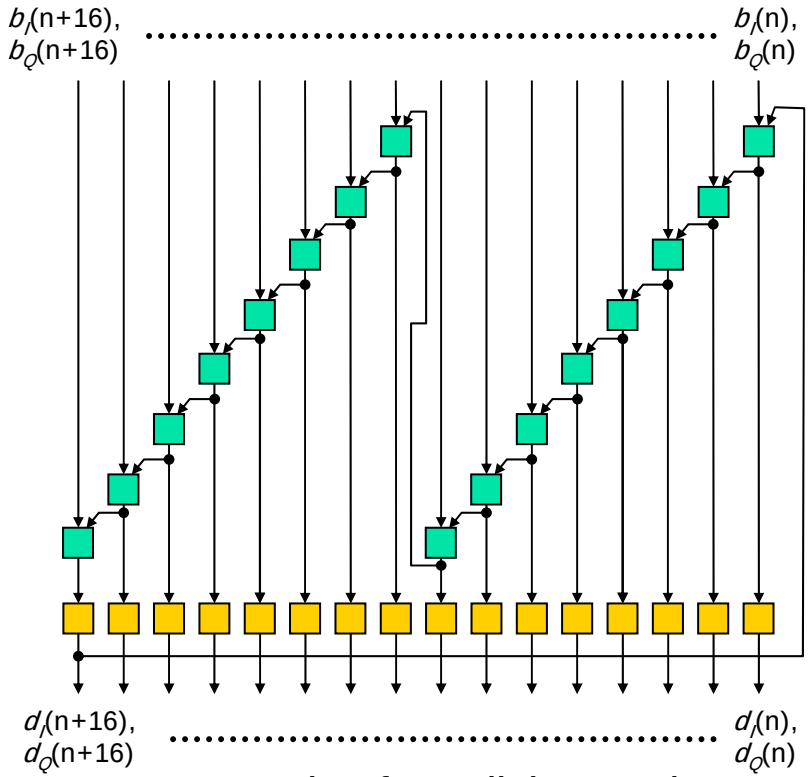
- Possible to speed up by parallel processing
- Speed-up technique for the adder-carry circuit is effective.



DQPSK



Serial precoder



Example of parallel precoder
(16 symbols in parallel; 32-bit width)

Experiments on parallel precoder implementation

- Tried to implement parallel precoder for DQPSK using FPGA and ASIC
  - Applied Han-Carlson adder-carry tree
- For FPGA (used Xilinx Virtex5LX)
  - 256 symbols in parallel; 512-bit width
    - 512 bits x 201.41 MHz = 103.125 Gbit/s
    - Used 2.4k LUTs and 3k FFs
      - Equivalent to 55k gates for ASIC (2-input NAND)

      -> Small FPGA
- For ASIC (used 90-nm process)
  - 128 symbols in parallel; 256-bit width
    - 256 bits x 402.83 MHz = 103.125 Gbit/s
    - Used 19k gates (2-input NAND)

      -> Small size (< 0.4-mm-square die)
- Easy to implement

LUT: Look-up Table
FF: Flip-flop