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Fiber Optic Solutions
for High-Speed Networks

XLAUI/CAUI TP4 VMA specification issue (Clause 83B)

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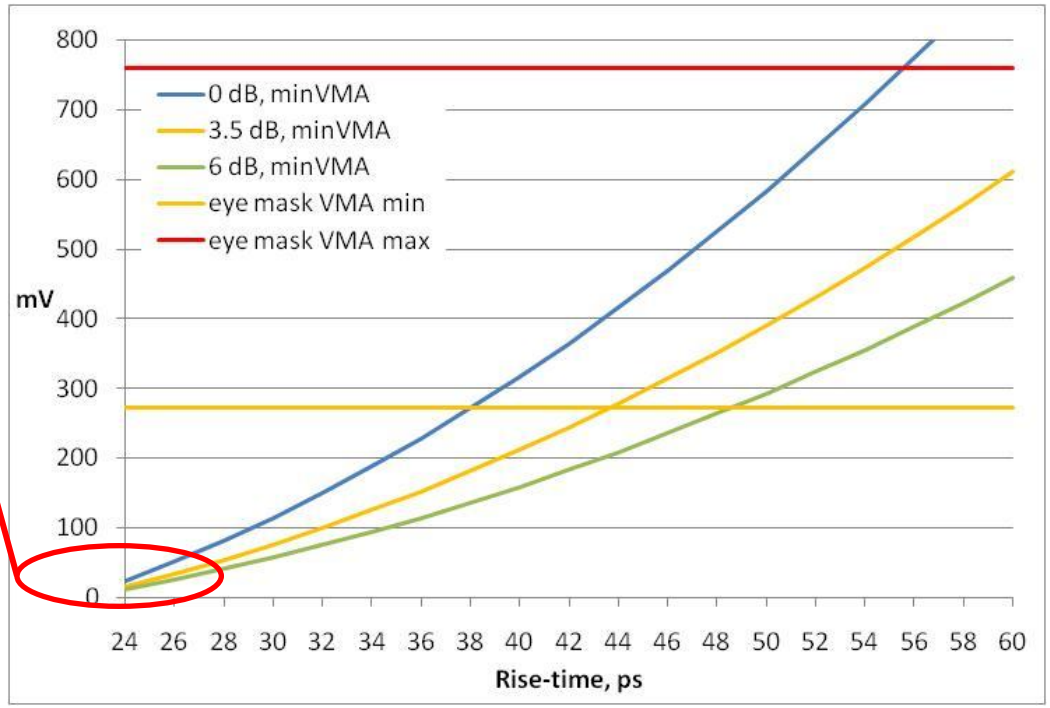
Minimum VMA spec in Clause 83B: the issue

- The Minimum VMA spec in table 83B-3 refers to equation 83B-6
- … it leads to unreasonably small values of VMA for fast rise-time (but 83B compliant) module XLAUI outputs.
- There needs to be an additional constraint on Minimum VMA specified in Clause 83B to limit the minimum VMA for fast ristime, high de-emphasis module XLAUI outputs.

$$\text{Minimum VMA (mV)} = (-110 - 2.13x + 0.32x^2) \times (10^{-y/20}) \qquad \text{(83B–6)}$$

where

x is the rise or fall time (whichever is larger) in ps
y is de-emphasis value in dB



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Analysis of host input signal tolerance spec in 83B and XLAUI link model

Table 83B–4—Specifications at host compliance points

Reference	Compliance point		Value	Unit
Host output signal specifications	HCB output	TP1a	See Table 83B–5	
Minimum host differential output return loss	HCB output	TP1a	See Equation (83B–7)	dB
Minimum host differential input return loss	HCB input	TP4a	See Equation (83B–7)	dB
Host input tolerance signal	MCB output	TP4	See 83B.2.3	

- 83B.2.3 defines a stressed eye test - added jitter and eye closure) *with no signal de-emphasis applied (as shown in figure 83B-9)*. The minimum eye opening is set by eye-mask coordinates to 272 mV p-p.
- The XLAUI chip to module link budget indicates this input signal is attenuated by up to 7.9 dB (e.g. for 1010 patterns), but VMA is relatively unchanged
- i.e. the inner eye at the host XLAUI chip input may be reduced by up to 7.9 dB, from 272 mV to 109 mV p-p
- To achieve the same level of eye opening at the host XLAUI chip input a 3.5 dB de-emphasis signal would need a VMA of 181 mV p-p
  - 181 mV reduced by (7.9 dB - 3.5 dB) is 109 mV
  - consistent with Equation 83B-6 with a minimum rise time of 36ps

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Minimum VMA spec: proposed solution

- Add a note to equation 83B-6 which says 'The minimum value which may be used in equation 83B-6 is 36ps, even if the rise or fall time is less than 36 ps'

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Back up

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Host XLAUI electrical specifications in 83B and 83A

- Host output: minimum VMA is 85 mV p-p
- Host input sensitivity is 85 mV p-p (at XLAUI chip input, see 802.3ba, figure 83A-2)
- Any fixed limit to minimum VMA (in addition to Equation 83B-6) should be consistent with this level of host XLAUI sensitivity

Table 83B–5—Host electrical output

Parameter	Subclause reference	Value	Units
Maximum output AC common-mode voltage, RMS	86A.5.3.1	20	mV
Minimum output rise and fall time (20% to 80%)	83A.3.3.2	24	ps
Maximum Total Jitter	83A.3.3.5	0.62	UI
Maximum Deterministic Jitter	83A.3.3.5	0.42	UI
Host electrical output eye mask definition X1	83A.3.3.5	0.31	UI
Host electrical output eye mask definition X2	83A.3.3.5	0.5	UI
Host electrical output eye mask definition Y1	83A.3.3.5	42.5	mV
Host electrical output eye mask definition Y2	83A.3.3.5	425	mV

Table 83A–2—Receiver characteristics

Parameter	Subclause reference	Value	Units
Signaling rate per lane (range)	—	10.3125 ± 100 ppm	GBd
Minimum input AC common-mode voltage tolerance, RMS	86A.5.3.1	20	mV
Minimum input rise and fall time tolerance (20% to 80%)	83A.3.3.2	24	ps
Differential input return loss	83A.3.4.3	See Equation (83A–7)	dB
Differential to common-mode input return loss	83A.3.4.4	See Equation (83A–8)	dB
Stressed receiver tolerance			
Minimum Total Input Jitter Tolerance	83A.3.4.2	0.62	UI
Minimum Deterministic Input Jitter Tolerance	83A.3.4.2	0.42	UI
Receiver eye mask definition X1	83A.3.4.2	0.31	UI
Receiver eye mask definition X2	83A.3.4.2	0.5	UI
Receiver eye mask definition Y1	83A.3.4.2	42.5	mV
Receiver eye mask definition Y2	83A.3.4.2	425	mV

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83B Module electrical specs and eye mask

Table 83B–3—Module electrical output

Parameter	Subclause reference	Value	Unit
Maximum differential output voltage, peak-to-peak	83A.3.3.1	760	mV
Minimum de-emphasis	83A.3.3.1	3.5	dB
Maximum de-emphasis	83A.3.3.1	6	dB
Minimum VMA	83A.3.3.1	See Equation (83B–6)	mV
Maximum termination mismatch at 1 MHz	86A.5.3.2	5	%
Maximum output AC common-mode voltage, RMS	86A.5.3.1	15	mV
Minimum output rise and fall time (20% to 80%)	83A.3.3.2	24	ps
Maximum Total Jitter	83A.3.3.5	0.4	UI
Maximum Deterministic Jitter	83A.3.3.5	0.25	UI
Module electrical output eye mask definition X1	83A.3.3.5	0.2	UI
Module electrical output eye mask definition X2	83A.3.3.5	0.5	UI
Module electrical output eye mask definition Y1	83A.3.3.5	136	mV
Module electrical output eye mask definition Y2	83A.3.3.5	380	mV

Implicit 272mV p-p minVMA for 0 dB de-emphasis, for 'worst case' rise-time

- Electrical eye-mask for module TP4 electrical output
  - (note: eye mask is a diamond shape, since X2=0.5)

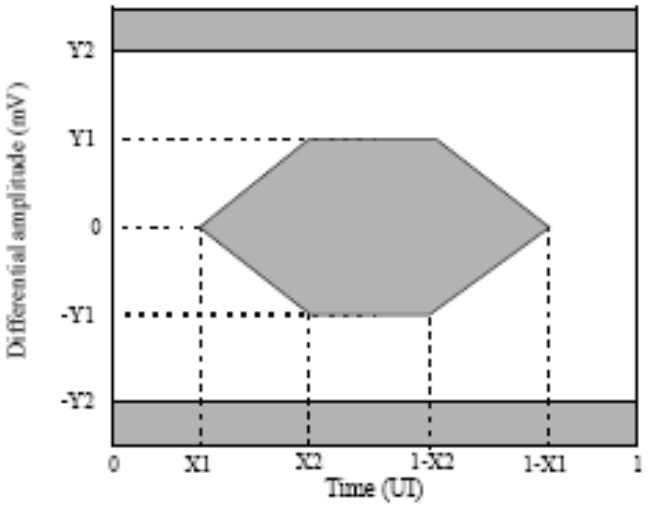

Figure 83A–8—Transmitter eye mask

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XLAUI link budget (Clause 83B)

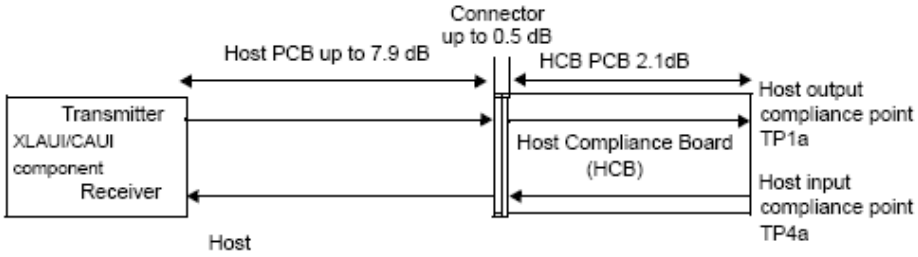

Figure 83B–4—Chip-module HCB insertion loss budget at 5.15625 GHz

Table 83B–1—Chip-module loss budget

Section	Differential insertion loss max. (at 5.15625 GHz)
Host XLAUI/CAUI component to connector	7.9 dB
Connector loss	0.5 dB
Connector to module XLAUI/CAUI component	2.1 dB

$$Insertion_loss(f) \le \begin{cases} 0.111 + 1.046\sqrt{f} + 1.05f & 0.01 \le f < 7 \\ -11.82 + 3.15f & 7 \le f \le 11.1 \end{cases} \text{ (dB)} \qquad (83B\text{–}1)$$

where

Insertion_loss(f) is the differential insertion loss at frequency *f*
f is the frequency in GHz

- XLAUI model of Host PCB has up to 7.9dB loss at 5.16GHz, 0.1dB loss at 0 Hz
  - high frequency signal components (e.g. 1010 pattern) attenuated by up to 7.9 dB
  - low frequency signal components (eg long sequences of '1' or '0') see little attenuation
  - the data '1' and '0' rails (≈VMA) are relatively unaffected by host PCB loss

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