

# PSE Startup Discussion

**Michael McCormack**  
**Texas Instruments**

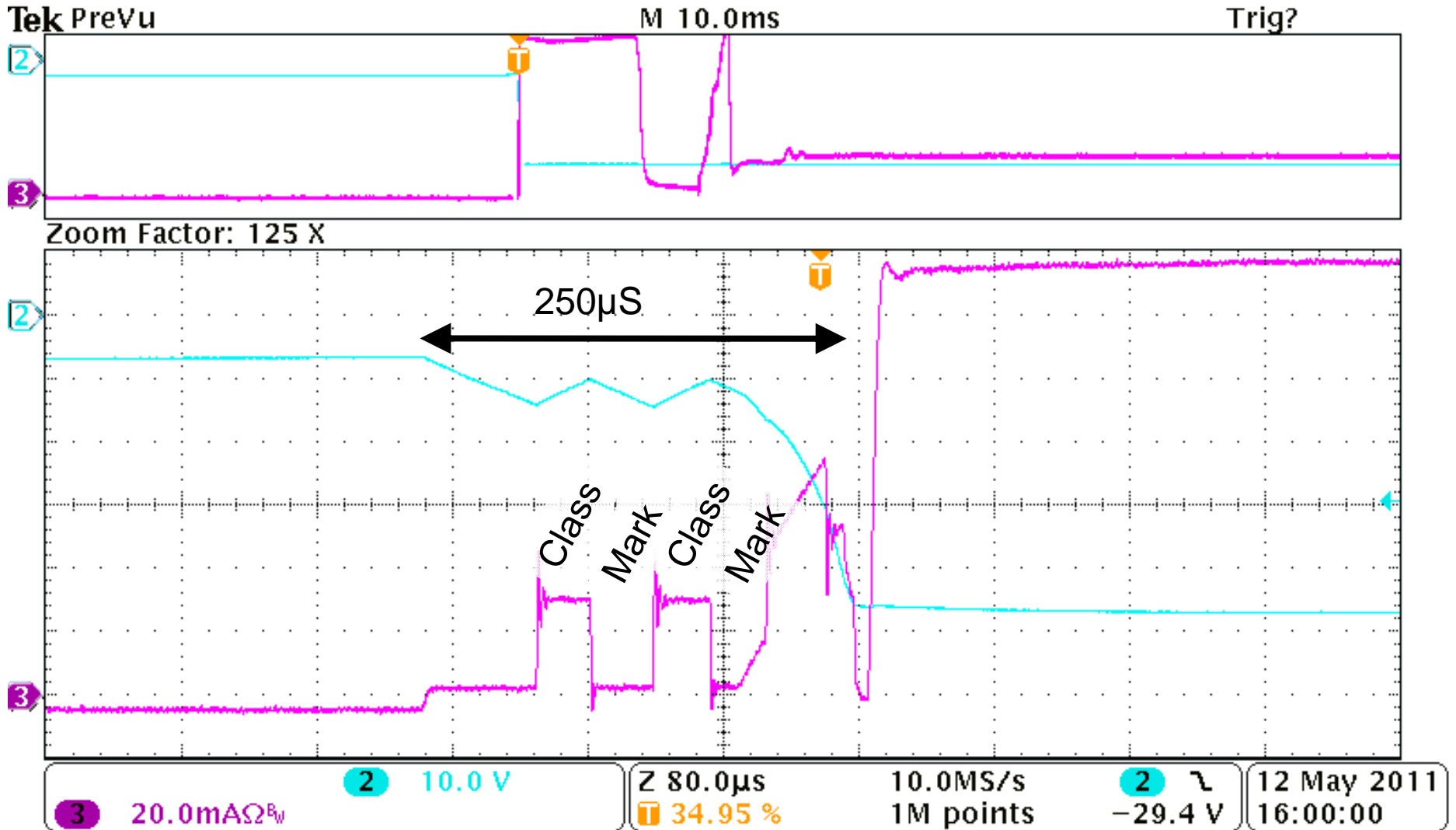
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# Overview

- A customer identified an interoperability issue between a TI PSE controller IC and a third party PD.
- Inoperability failure was found to be caused by PSE voltage fluctuations which are interpreted by the PD as a Layer 1 Type 2 acknowledge.
- Review of the IEEE specification has led to additional questions regarding legacy device interoperability and present PSE requirements.
- Testing with additional PDs has shown at least one other PD is susceptible with the TI PSE; I have not tested other PSE controllers.

# TI PSE and Third Party PD



# IEEE Specifications

- IEEE Std 802.3af through 802.3-2008 allowed 1ms of settling in section 33.2.8.5.
- IEEE Std 802.3at, without settling time (now 33.2.7.5), was published Oct 30, 2009.

IEEE  
Std 802.3-2008

REVISION OF IEEE Std 802.3:

## 33.2.8.5 Output current in startup mode

The specification for  $I_{inrush}$  in Table 33-5 shall be met under the following conditions:

- For duration of 50 ms min, duty cycle = 5% min.
- Measurement to be taken after 1 ms to ignore startup transients.
- During startup, the minimum  $I_{inrush}$  requirement applies for duration  $t_{inrush}$ .
- During startup, for PI voltages above 30 V, the minimum  $I_{inrush}$  requirement is as specified in Table 33-5, item 5.
- During startup, for PI voltages between 10 V and 30 V, the minimum  $I_{inrush}$  requirement is 60 mA. See Figure 33C.4 and Figure 33C.6.

## 33.2.7.5 Output current in POWER\_UP mode

POWER\_UP mode occurs between the PSE's transition to the POWER\_UP state and either the expiration of  $T_{inrush}$  or the conclusion of PD inrush currents (see 33.3.7.3). However, for practical implementations, it is recommended that the POWER\_UP mode persist for the complete duration of  $T_{inrush}$ , as the PSE may not be able to correctly ascertain the conclusion of a PD's inrush behavior.

The PSE shall limit the maximum current sourced at the PI during POWER\_UP. The maximum inrush current sourced by the PSE shall not exceed the PSE inrush template in Figure 33-13.

- During POWER\_UP, for PI voltages between 0 V and 10 V, the minimum  $I_{inrush}$  requirement is 5 mA.
- During POWER\_UP, for PI voltages between 10 V and 30 V, the minimum  $I_{inrush}$  requirement is 60 mA.
- During POWER\_UP, for PI voltages above 30 V, the minimum  $I_{inrush}$  requirement is as specified in Table 33-11.

- b) Measurement to be taken after 1ms to ignore startup transients.

- The PSE IC in question was released June 16, 2009.

# Summary

- 802.3at may have caused previously compliant equipment to be non-compliant.
- PSE startup voltage fluctuations are not precluded by 802.3at.
- PDs which have demonstrated interoperability problems are compliant to 802.3at.
  
- Compliant devices which do not interoperate are not good.
  
- I expect to submit a comment against 33.2.7.5 to the effect of:
  1. Add allowance for 1ms voltage fluctuation at PSE start.
  2. Require “monotonically increase” of port voltage after 1ms.
  3. Add a NOTE in the PD section about problems with PSEs during startup.
  
- I would appreciate off line conversations.