

-----+  
| 8802-3/802.3 REVISION REQUEST 1113 |  
+-----+

DATE: 17th September, 2003  
NAME: Peter Bradshaw  
COMPANY/AFFILIATION: BitBlitz Communications  
E-MAIL: pbradshaw@bitblitz.com

REQUESTED REVISION:  
STANDARD: IEEE Std. 802.3ae-2002  
CLAUSE NUMBER: 45.2.3 (see proposed revision for details)  
CLAUSE TITLE: PCS registers

PROPOSED REVISION TEXT:

1a. In 45.2.3.1.2:

INSERT BEFORE: For all other port types when operating at 10 Gb/s, the PCS loopback functionality is not applicable and writes to this bit shall be ignored and reads from this bit shall return a value of zero.

THIS: For 10GBASE-X port types when operating at 10 Gb/s, the PCS loopback functionality is optional. If implemented, this bit may set a loopback mode of operation. If loopback is not implemented, writes to this bit shall be ignored and reads from this bit shall return a value of zero.

1b. In 45.2.3.9:

REPLACE: Table 45-36, replace 3.24.10:4 by 3.24.9:4, and add a new row above with:

3.24.10	Loopback Capability
1	= 10GBASE-X PCS has the ability to perform a loopback function
0	= 10GBASE-X PCS does not have the ability to perform a loopback function

RO

For details see attached draft.

RATIONALE FOR REVISION:

802.3ae-2002 Section 44A7 (including Figure 44A-7) implies a possible loopback ability at all of the PMA, WIS and PCS sublayers (explicitly omitting WIS if not present). Other parts of 802.3ae specify:-

- A.) PMA loopback (45.2.1.1.4) is mandatory or optional, depending on the PMA type, the ability being advertised in bit 1.8.0;
- B.) PCS loopback is mandatory for a 10G-BASE-R PCS, but is forbidden for all other PCS types (45.2.3.1.2). However, a device incorporating WIS is expected to incorporate or involve a 10GBASE-R PCS as well, so some level of PCS loopback is likely to be provided there as well. In particular, the assertion that such a loopback is 'not applicable' seems an unnecessary and unproductive restriction.

The proposed changes remove the prohibition against loopback in a 10GBASE-X PCS device, making it optional. If present, the 3.24.10 bit can

be used to advertise its presence, since this register is required in a 10GBASE-X PCS, and the bit usage corresponds to that used in some XGXS devices without conflict.

IMPACT ON EXISTING NETWORKS:

Current compliant devices are still in compliance, since they do not have the loopback\* and the advertising bit would say so. A system that did not expect to utilize such a loopback probably ignores bit 3.24.10 in any case (it should), and will not set bit 3.0.14, and a system that does will determine from 3.24.10 whether it may.

\*Side bet: I suspect many do, but implement it via some other mechanism, such as via a vendor-specific register.

```
+-----+
| Please attach supporting material, if any
| Submit to:- Bob Grow, Chair IEEE 802.3
|           E-Mail: Bob.Grow@intel.com
|
|           +----- For official 802.3 use -----+
|           | REV REQ NUMBER: 1113
|           | DATE RECEIVED: 17th September, 2003
|           | EDITORIAL/TECHNICAL
|           | ACCEPTED/DENIED
|           | BALLOT REQ'D YES/NO
|           | COMMENTS: 29-Sep-04 Ver: D1.1 Status: W
|
+-----+
| For information about this Revision Request see -
| http://www.ieee802.org/3/maint/requests/revision\_history.html#REQ1113
+-----+
```

### 45.2.3.1.2 Loopback (3.0.14)

Change the first paragraph of subclause 45.2.3.1.2 as follows:

The 10GBASE-R PCS shall be placed in a Loopback mode of operation when bit 3.0.14 is set to a one. When bit 3.0.14 is set to a one, the 10GBASE-R PCS shall accept data on the transmit path and return it on the receive path. The specific behavior of the 10GBASE-R PCS during loopback is specified in 49.2. For 10GBASE-X port types when operating at 10 Gb/s the PCS loopback functionality is optional. If implemented, this bit may set a loopback mode of operation. If loopback is not implemented, writes to this bit shall be ignored and reads from this bit shall return a value of zero. For all other port types when operating at 10 Gb/s, the PCS loopback functionality is not applicable and writes to this bit shall be ignored and reads from this bit shall return a value of zero.

### 45.2.3.9 10GBASE-X PCS status register (Register 3.24)

Change Table 45-37 of subclause 45.2.3.9 as follows:

**Table 45–37—10GBASE-X PCS status register bit definitions**

Bit(s)	Name	Description	R/W <sup>a</sup>
3.24.15:13	Reserved	Ignore when read	RO
3.24.12	10GBASE-X lane alignment status	1 = 10GBASE-X PCS receive lanes aligned 0 = 10GBASE-X PCS receive lanes not aligned	RO
3.24.11	Pattern testing ability	1 = 10GBASE-X PCS is able to generate test patterns 0 = 10GBASE-X PCS is not able to generate test patterns	RO
<u>3.24.10</u>	<u>Loopback Capability</u>	<u>1 = 10GBASE-X PCS has the ability to perform a loopback function</u> <u>0 = 10GBASE-X PCS does not have the ability to perform a loopback</u>	<u>RO</u>
3.24.9:4	Reserved	Ignore when read	RO
3.24.3	Lane 3 sync	1 = Lane 3 is synchronized 0 = Lane 3 is not synchronized	RO
3.24.2	Lane 2 sync	1 = Lane 2 is synchronized 0 = Lane 2 is not synchronized	RO
3.24.1	Lane 1 sync	1 = Lane 1 is synchronized 0 = Lane 1 is not synchronized	RO
3.24.0	Lane 0 sync	1 = Lane 0 is synchronized 0 = Lane 0 is not synchronized	RO

<sup>a</sup>RO = Read Only