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| 8802-3/802.3 REVISION REQUEST 1147 |  
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DATE: 21st May, 2004  
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REQUESTED REVISION:  
STANDARD: IEEE Std 802.3-2002  
CLAUSE NUMBER: Table 14-2  
CLAUSE TITLE: Maximum timing parameters

PROPOSED REVISION TEXT:

Change text from "RD\_input" to "*RD\_input*" by adding italic attribute to text "RD\_input".

Change text from "output" to "*output*" by adding italic attribute to text "output".

Change text from "signal\_quality\_error" to "*signal\_quality\_error*" by adding italic attribute to text "signal\_quality\_error".

For details see attached draft.

RATIONALE FOR REVISION:

Text should be in italics.

IMPACT ON EXISTING NETWORKS:

Editorial change only.

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| Please attach supporting material, if any |  
| Submit to:- Bob Grow, Chair IEEE 802.3 |  
| E-Mail: Bob.Grow@intel.com |  
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| +----- For official 802.3 use -----+ |  
| REV REQ NUMBER: 1147 |  
| DATE RECEIVED: 21st May, 2004 |  
| EDITORIAL/~~TECHNICAL~~ |  
| ACCEPTED/~~DENIED~~ |  
| BALLOT REQ'D YES/~~NO~~ |  
| COMMENTS: 08-Mar-06 Ver: D2.0 Status: P |  
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| For information about this Revision Request see - |  
| [http://www.ieee802.org/3/maint/requests/revision\\_history.html#REQ1147](http://www.ieee802.org/3/maint/requests/revision_history.html#REQ1147) |

Replace Table 14-2 with the following (Summary of changes - in M3 change 'RD\_input' to read 'RD\_input', 'output' to read 'output' and 'signal\_quality\_error' to read 'signal\_quality\_error', in M8 change 'signal\_quality\_error' to read 'signal\_quality\_error'):

**Table 14–2—Maximum timing parameters**

Symbol	Function	Bit Loss <sup>a</sup>	Invalid Bits <sup>b</sup>	Steady-State Propagation Delay <sup>b</sup>	Start-up Delay <sup>b</sup>		Specified in
					Maximum	Variability	
M1	<i>RD_input</i> to <i>input</i> on DI	5.0	1.0	2.0	8.0	2.0	14.2.1.2
M2	<i>output</i> on DO to <i>TD_output</i>	2.0	1.0	2.0	5.0	2.0	14.2.1.1
M3	<i>RD_input</i> * <i>output</i> to <i>signal_quality_error</i>	—	—	—	9.0	—	14.2.1.4
M4	<i>RD_idle</i> + <i>output_idle</i> (end of collision) to <i>mau_available</i>	—	—	—	9.0	—	14.2.1.4
M5	<i>RD_input</i> * <i>output</i> to <i>input</i> on DI from circuit RD	—	—	—	9.0	—	14.2.1.4
M6	<i>RD_idle</i> * <i>output</i> to <i>input</i> on DI from circuit DO	—	—	—	9.0	—	14.2.1.4
M7	<i>output_idle</i> on DO to <i>signal_quality_error</i>	—	—	—	6 < x < 16	—	14.2.1.5
M8	<i>signal_quality_error</i> duration for SQE test	—	—	—	5 < x < 15	—	14.2.1.5
M9	<i>output</i> on DO to <i>input</i> on DI	5.0	1.0	1.0	7.0	—	14.2.1.3
T1	twisted-pair propagation	0	0	10.00	10.00	—	14.4.2.4
A1	AUI cable propagation (50 m)	0	0	2.57	2.57	—	7.4.3.7

<sup>a</sup>All time in BT.

<sup>b</sup>For an explanation of the meaning of variability, see 14.2.1.1 and 14.2.1.2.

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