8802-3/802.3 REVISION REQUEST 1167

DATE: 30th March, 2005
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REQUESTED REVISION:
STANDARD: IEEE Std. 802.3af-2003
CLAUSE NUMBER: Figure 33-6
CLAUSE TITLE: PSE State diagram

PROPOSED REVISION TEXT:

Add new variable option_vport30 to 33.2.3.4. It will be an optional variable. Change state diagram (figure 33-6) per the attached drawing.

option_vport30
This variable is indicating PSE port voltage.
Values:
False: Vport is above 30V.
True: Vport is below 30V.
Tlim minimum may be shorten to 1ms.

RATIONALE FOR REVISION:

The state diagram allows a scenario that violates the minimum requirement of Ted as specified in table 33-5 item 21 when PSE-PD motor-boating or oscillates with high peak power during short circuit condition.

The proposed revision allows the option of preventing such scenarios.

Problem description:

During short circuit condition, PD input voltage is dropping below Voff=30V (table 33-12 item 8) the PD enters to its OFF mode and the PD input capacitor is discharged partially or completely pending the short circuit condition duration.

Now the current is very low so the PSE voltage is going high again and when crosses the PD Von value (30V to 42) it charge the PD capacitor again by drawing Iinrush.

The PSE voltage will drop again below Voff of the PD (30V) and the process will be repeated until TLIM is done.

The results of this scenario are:

1. The time between the first startup to the 2nd is much below Ted=750ms which violates spec requirements of keeping cool off time between consecutive startups.

It should be noted that while PSE is in POWER_APPLIED status, the PD is in OFF or Startup state that's why Ted can not be controlled (From system point of view, there is no synchronization between PSE state and PD state).

Effectively the PSE may faces multiple inrush time duration which is 50ms minimum. According to the state diagram, Tlim starts counting once I>Iinrush and nothing can stop the counter until 50ms to 75ms time is reached. This scenario may generate excessive heat which should have been prevented by Ted minimum value 750mS as explained above.

2. Until TLIM timer done, the PSE and PD will pass few consecutive cycles of startups which as function of the short circuit time duration and the status of the PD during short will cause PSE-PD motor boating at high peak power, may generating noise and in some cases will cause PSE-PD stability issues due to the fact that the PSE during short circuit is a current source with high impedance that drives negative input impedance of the PD DC/DC if PD is ON and PSE still in current limit.

3. In addition, to prevent shutting down the port for short transients, it is recommended to set 1ms minimum value for Tlim.

In order to handle this scenario, we need to allow to shut the PSE port if Vport is below a value that cause PD to be at OFF.

Such Vport value exist in the spec, the 30V border line in the PD spec which is Voff per table 33-12 item 8 .

Using this optional variable in the state diagram will fix the problem by changing the inputs to ERROR_DELAY_SHORT state from: tlim_timer_done to: Tlim_timer_done + !tlim_timer_done*option_vport30*power_applied

IMPACT ON EXISTING NETWORKS:

None if the new variable is optional as proposed.

Please attach supporting material, if any		
Submit to:- Bob Grow, Chair IEEE 802.3		
E-Mail: Bob.Grow@intel.com		
+------- For official 802.3 use ----------+		
REV REQ NUMBER: 1167		
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For information about this Revision Request see -		
http://www.ieee802.org/3/maint/requests/revision_history.html#REQ1167		

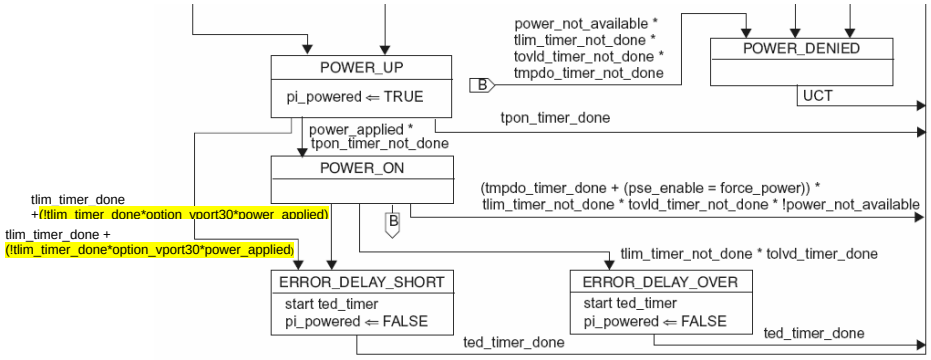

Figure 33–6—PSE state diagram