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| 8802-3/802.3 REVISION REQUEST |
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DATE: 21-May-2017
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REQUESTED REVISION:
  STANDARD: IEEE Std 802.3-2015
  CLAUSE NUMBER: 33
  CLAUSE TITLE: DTE Power via MDI

PROPOSED REVISION TEXT:

[1] The equation on the transition from the MDI_POWER1 state to the MDI_POWER_DLY state in Figure 33-31 'Type 1 and Type 2 PD state diagram' be changed to read '(pse_power_type = 2) + (pse_dll_power_type = 2 * pd_dll_ready)'.

[2] The assignment 'pse_dll_power_type <= pse_power_type' in the INITIALIZE state in Figure 33-49 'PD power control state diagram' be removed.

[3] The definition of pse_power_type be removed from 33.5.3.3 'Single-signature system Variables'.

[4] The definition of pse_dll_power_type be removed from 33.5.3.3 'Single-signature system Variables'.

[5] In definition of pse_dll_power_type in subclause 33.3.3.4 'Type 1 and Type 2 Variables' change the text 'A control variable output by the PD power control state diagram (Figure 33-49) that ...' to read 'A variable mapped from the aLldpXdot3RemPowerType as defined in Table 33-41 that indicates ...'.

RATIONALE FOR REVISION:

There is an assignment to the pse_dll_power_type variable in the INITIALIZE state of Figure 33-49 'PD power control state diagram' as well as a mapping to it in Table 33-41 'Attribute to state diagram variable cross-reference' so effectively there are two sources to this variable. There is a case where a Type 2 PD is connected to a Type 2 PSE that supports 1-event physical layer classification, Data Link Layer Classification which will result in two different values for pd_dll_power_type from these two sources.

On entry to the DO_DETECTION state of Figure 33-31 'Type 1 and Type 2 PD state diagram' the pse_power_type variable is set to 1. As a result of the 1-event physical layer classification that this PSE will perform, the state diagram will then progress to the DO_CLASS_EVENT1 state and then, assuming that the PSE starts supplying power, will progress to the MDI_POWER1 state once the power_received variable becomes TRUE.

The pd_max_power variable will be set to 0 (4 modulo 4), allowing

the PD to draw up to Class 0 power (13.0W). Since pse_power_type has been set to 1 the state diagram will then progress to the DLL_ENABLE state setting the pd_dll_enabled variable to TRUE enabling Data Link Layer Classification for the PD. At this point however pse_power_type is still set to 1 so the state diagram will transition back to the MDI_POWER1 state where it will remain as pd_dll_enabled is now TRUE.

Since the PSE supports Data Link Layer Classification the aLldpXdot3RemPowerType attribute within the oLldpXdot3RemSystemsGroup managed object class will return a bit string indicating a Type 2 PSE at some point afterwards when the pd_dll_ready variable becomes TRUE. This, according to Table 33–41 'Attribute to state diagram variable cross-reference', also results in pd_dll_power_type being set to 2. The problem is that, according to the Figure 33-49 'PD power control state diagram', when pd_dll_ready becomes TRUE the value of pse_power_type is latched on to pse_dll_power_type, and at that point in time it is 1.

Now it seems that the intent was that when pse_dll_power_type became 2 due to Data Link Layer Classification, the equation on the transition from MDI_POWER1 to MDI_POWER_DLY state became true (pse_power_type = 2) + (pse_dll_power_type = 2) causing, after a delay, entry to the MDI_POWER2 state. At that point the pd_max_power variable will be increased from 0 (class_sig modulo 4) to 4 due to the assignment pd_max_power <= class_sig enabling the power drawn to increase from Type 1 to Type 2 limits.

The problem is there are two values of pse_dll_power_type once Data Link Layer Classification is in operation, the one based on the Table 33–41 mapping which in this case would be set to a value of 2, and the one output by the Figure 33-49 state diagram, which in this case would be set to a value of 1. As well as the statement that 'State diagrams take precedence over text.' the definition of the pse_dll_power_type variable in subclause 33.3.3.4 'Type 1 and Type 2 Variables' for Figure 33-31 states 'A control variable output by the PD power control state diagram (Figure 33–49) that ...'. . Based on this it would seem that the latter value of 1 should be used, however the problem with this is that the MDI_POWER2 state will then never be reached, and the PD will have to continue draw power within the Type 1 limits.

It would seem a better approach would be to remove the assignment of pse_power_type to pse_dll_power_type in the INITIALIZE state of Figure 33–49 'PD power control state diagram' and just use the Table 33–41 'Attribute to state diagram variable cross-reference' mapping for Figure 33-31. This is the only use of the pse_power_type and pse_dll_power_type variables in Figure 33–49 so they can also be removed from the associated variable definition lists.

The variable pse_dll_power_type however has to gated while pd_dll_ready is FALSE, since at that time aLldpXdot3RemPowerType is undefined and therefore the mapping of Table 33–41 'Attribute to state diagram variable cross-reference' is undefined. Based on this the use of pse_dll_power_type on the MDI_POWER1 to MDI_POWER_DLY transition should be qualified with pse_dll_ready = TRUE, so the equation would become (pse_power_type = 2) + (pse_dll_power_type = 2

* pd_dll_ready).

IMPACT ON EXISTING NETWORKS:

None. This change will clarify the source of pse_dll_power_type in a Type 2 PD. Type 2 PDs will have had to have been implemented using the suggested source, if not a PD would not have been able to draw power in excess of the Type 1 limit from a Type 2 PSE with 1-event physical layer Classification and Data Link Layer Classification.

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	REV REQ NUMBER: 1307		
	DATE RECEIVED: 21st May, 2017		
	EDITORIAL/TECHNICAL		
	ACCEPTED/DENIED		
	BALLOT REQ'D YES/NO		
	COMMENTS:		
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