January 18, 2018

To: David Law and members of the IEEE 802.3 Working Group
cc: Peter Anslow, 802.3 WG Secretary
John D'Ambrosia – Beyond 10km Optical PHYs Study Group Chair

Subject: 400ZR Interop Project

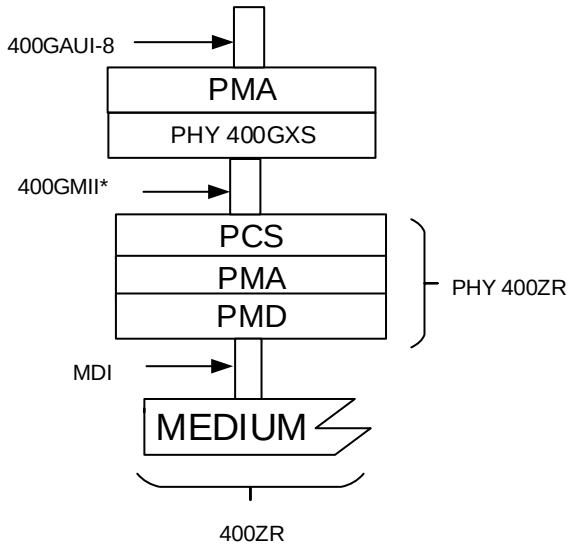
From: Klaus-Holger Otto, OIF Technical Committee Chair (klaus-holger.otto@nokia.com)

Dear Mr. Law and members of IEEE 802.3,

Thank you for your Liaison letter dated November 9th 2017. We appreciate your interest in the 400ZR project. The PLL WG held an interim meeting on Monday January 15th, which was then followed up with several work sessions during the Q1 18 Technical and MA&E Committee meetings held on the 16th through the 18th in San Antonio TX. During one of the work sessions we were able to review your inputs and provide the following responses and further updates:

Your recommendation: "Given the efforts to define 400ZR as an Ethernet PHY, we would recommend using the abstraction approach used for Ethernet standards, and changing the "to/from 400ZR PCS" at the bottom of the diagram to "400GMII." It was also noted that instead of labeling the overall figure as "400G PCS (partial processes)" you might label it as "400G PHY XS," which was stated in the paragraph prior to the block diagram to describe it."

An abstraction approach to the functional block diagram is represented below:




*Logical Equivalent Implementation - The rate matching functions shall be disabled to/from the 400GMII interface in both directions. No Idle deletion/insertion shall be performed.

GMP is baselined for the following reasons:

1) Desire to support both frequency and data transparency including preservation of IFG, while maintaining +/- 100ppm tolerance for 400GbE. This will also allow us to support FlexE directly.
2) GMP has been used in multiple generations of OTN products to carry Ethernet. Supporting GMP requires a small logic footprint.
3) Asynchronous mapping effectively decouples the timing of the system-side interface from the line. For a high speed coherent interface it is critical to minimize phase noise. Isolating the clocks eliminates the jitter transfer contribution of a cascaded fractional PLL locked to the host generated interface.
4) GMP mapping can work equally well with a line-side interface of +/-100ppm. The choice of +/- 20ppm is based on market opportunity and addresses other protocols that may require +/- 20ppm in the future. The choice by OIF does not restrict other organizations from using the same 400ZR framing with +/-100ppm on the line-side.

During the San Antonio meeting the full datapath from the 400GAUI-8 to the 400ZR line was fully defined. OIF2017.245.06 was adopted as the 400ZR IA baseline. The optical parameters and distance supported by (passive) single channel ZR are not currently baselined.

We will continue to update the IEEE 802.3 Working Group on the progress on 400ZR IA. Our next meeting is in Nuremberg Germany, April 23rd - 27th, 2018.

Sincerely,

Klaus-Holger Otto
OIF Technical Committee Chair (klaus-holger.otto@nokia.com)