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LIAISON STATEMENT

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Title: LS on Timestamping Point for Multilane Ethernet Interfaces

LIAISON STATEMENT

For action to: IEEE 802.3

For comment to: -

For information to: IEEE 1588

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ITU-T Q13/15 is currently working on the transport of phase and time through packet networks using PTP defined in IEEE1588. One issue that has been raised recently is the timestamp point for multilane Ethernet interfaces, such as are required for 40G and 100G Ethernet (e.g. 4 x 10G lanes or 10 x 10G lanes).

Reconstruction of the data stream from such interfaces involves a de-skewing step, since each lane may have a different delay. The delay introduced by the de-skewing step is adaptive and hence unpredictable, but our understanding is that the magnitude of this lane skew can be up to 180 ns according to Table 80-5 of IEEE 802.3.

Q13/15's understanding of the problem is described in Appendix I.

The concern is that this may contribute to time-stamp error, or conceivably to delay asymmetry if the de-skewing delay is different in each direction. The asymmetry issue is of particular concern, since this creates a time error in the time distributed by PTP which the protocol is unable to correct or detect.

It would be of great benefit for the growing interest in the use of PTP, both in telecom applications and the many other industries using PTP, if a consistent time-stamping point could be defined for multilane interfaces, such that the potential for timestamp error and delay asymmetry is minimized.

Therefore Q13/15 invites IEEE802.3 to consider this issue as part of your ongoing work on Ethernet standardization.

Appendix I

PTP Timestamping on a Multi-Lane Interface

High data rate interfaces such as 40 and 100G typically use multi-lane interfaces, such as N x 10G or N x 25G lanes. These lanes may be distributed on separate fibres (e.g. 40GBASE-SR4) or separate wavelengths (e.g. 40GBASE-LR4).

Reconstruction of the data stream from such interfaces involves a de-skewing step, since each lane may have a different delay. This is because the fibres may have different physical lengths, or in the case of wavelengths, each wavelength propagates down the fibre at a different speed. The delay introduced by the de-skewing step is adaptive and hence unpredictable. Therefore this may contribute to time-stamp error, or conceivably to asymmetry if the de-skewing delay is different in each direction.

This could generate time error in PTP connections across such multi-lane interfaces.

Operation of Multi-Lane Interfaces

The following diagram shows the nature of the problem:

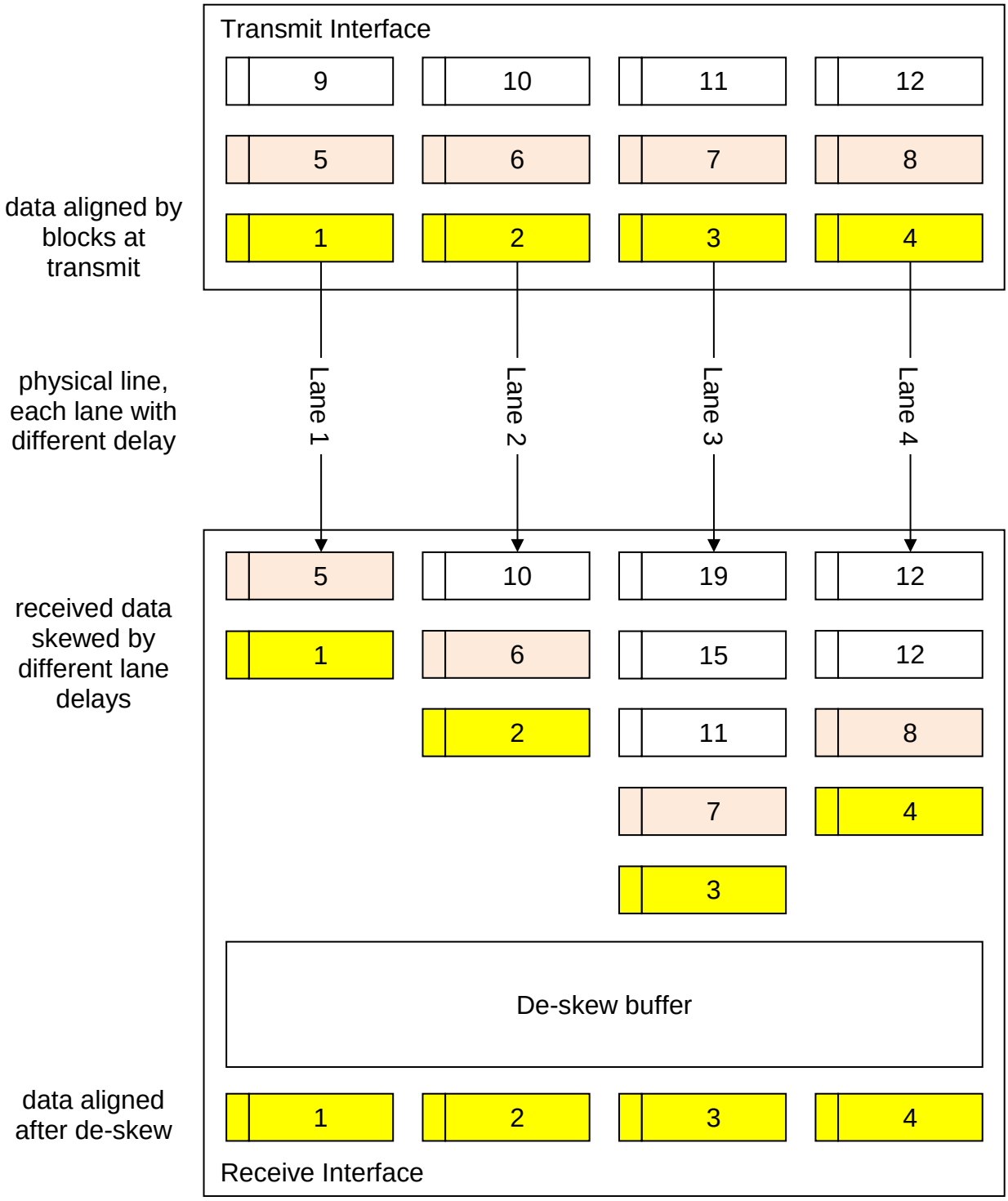

Figure 1: Multi-Lane Interface Lane Delay Skew

In the transmit interface, the data is transferred in blocks consecutively on each lane. The start-of-frame indicator may be transmitted on any of the lanes. This means that if the start-of-frame for a PTP message is transmitted on lane 1, the next PTP message could be transmitted starting on lane 2, and experience a different delay through the fibre. This magnitude of this lane skew can be up to 180ns according to Table 80-5 of IEEE 802.3.

Effect on Timing

There are two options for the time-stamping point in a multi-lane interface:

1. Time-stamping at the lane
   For best accuracy, PTP messages are normally time-stamped as close to the line as possible. With a multi-lane interface, that means time-stamping immediately as it comes off the lane. However, since each lane has a different delay, this will mean variation of up to 180ns depending on the lane used for the start-of-frame indicator.
   As the delays are normally constant (excluding thermal variations), it is likely that a histogram of PTP message delays will show several discrete values, one corresponding to each lane.

2. Time-stamping after the de-skew buffer
   The advantage of this is that the delay from transmit to the output of the de-skew buffer should be the same for each lane. However, it is unknown what the delay introduced by the de-skew buffer actually is.
   The issue here is that in the reverse direction there will also be a de-skew buffer of unknown delay. If the two de-skew buffers introduce different delays, this will cause asymmetry in the message delays in each direction. Time synchronization clocks requirement is 50ns or 20ns for the constant time error. Clearly a de-skew buffer that may be up to 180ns long could potentially introduce a constant time error larger than these limits.

Neither of these two options will give consistent results, especially as the receive interfaces may use different techniques depending on the manufacturer of the equipment and the components used. A consistent approach is required so that every manufacturer approaches this in the same way, otherwise the time error introduced by multi-lane interfaces will be too large to meet the budget allocations defined by Q13/15.

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