IEEE 802.3 100 Gb/s per Lane Electrical Interfaces and Electrical PHYs (100GEL) Study Group Opening Report

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IEEE 802.3 100 Gb/s per Lane Electrical Interfaces and Electrical PHYs Study Group information

Study Group Organization

Beth Kochuparambil, Study Group Chair

Kent Lusted, Recording Secretary

Study Group charter

Develop a PAR and CSD responses for “100Gb/s per Lane for Electrical Interfaces and Electrical PHYs”

Study Group Web Page

http://www.ieee802.org/3/100GEL/reflector.html

Study Group Reflector

http://www.ieee802.org/3/100GEL/index.html

Activities since CFI (November 2017, plenary)

Met for 1 interim meeting and 5 ad hoc teleconferences

- Geneva interim – http://www.ieee802.org/3/100GEL/public/18_01/index.html
- Ad hocs – http://www.ieee802.org/3/100GEL/public/adhoc/index.html

Interim Study Group meeting in January 2018, Geneva

- Reviewed 18 presentations
- 6 straw polls, 10 motions
- Adopted Objectives, CSD, and PAR
  - http://www.ieee802.org/3/100GEL/P802_3ck_Objectives_2018jan.pdf
  - https://mentor.ieee.org/802-ec/dcn/18/ec-18-0016-01-00EC-ieee-p802-3ck-draft-csd.pdf
  - https://mentor.ieee.org/802-ec/dcn/18/ec-18-0015-01-00EC-ieee-p802-3ck-draft-par.pdf
- Pre-submitted PAR and CSD for WG and EC feedback

Adopted Objectives (1 of 2)

5 Foundational Objectives

- Support a MAC data rate of 100 Gb/s, 200 Gb/s and 400 Gb/s
- Support full-duplex operation only
- Preserve the Ethernet frame format utilizing the Ethernet MAC
- Preserve minimum and maximum FrameSize of current IEEE 802.3 standard
- Support the existing bit error ratios (BERs) at the MAC/PLS service interface (or the frame loss ratio equivalent) for 100 Gb/s, 200 Gb/s and 400 Gb/s Ethernet

Adopted Objectives (2 of 2)

12 PHY/Interface Objectives (4 at each speed: single-lane, two-lane, four-lane)

- Define a single-lane 100 Gb/s Attachment Unit interface (AUI) for chip-to-module applications, compatible with PMDs based on 100 Gb/s per lane optical signaling
- Define a single-lane 100 Gb/s Attachment Unit Interface (AUI) for chip-to-chip applications
- Define a single-lane 100 Gb/s PHY for operation over electrical backplanes supporting an insertion loss ≤ TBD dB at TBD GHz.
- Define a single-lane 100 Gb/s PHY for operation over twin-axial copper cables with lengths up to at least TBD m.

Plan for the Week – 100GEL Study Group

Meeting Wednesday 10:30am-6pm & Thursday 8am-noon

- Grand Ballroom H

Goals for the meeting

- Review technical presentations
- Review/refine/fill in TBDs and current Objectives
- Consider feedback on pre-submitted CSD/PAR
- Update CSD/PAR

In 802.3WG Closing Plenary

- Request approval on documentation (Objectives, CSD, PAR)

Questions?

Thank you!