IEEE 802.3 Ethernet Working Group Liaison Communication

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Subject:	Liaison response to ITU-T Study Group 15 on timestamping point for multilane Ethernet interfaces	
Approval:	Agreed to at IEEE 802.3 Interim meeting, Bonita Springs, FL, USA, 17 September 2015	

Dear Mr Trowbridge, Mr Ruffini, and members of ITU-T SG15,

The IEEE 802.3 Ethernet Working Group would like to thank ITU-T Q13/15 for its liaison letter regarding "Timestamping Point for Multilane Ethernet Interfaces," dated 6th March 2015.

IEEE Std 802.3 defines path data delay registers for each MDIO Manageable Device (MMD) that forms a Physical Layer entity (PHY). A total of four values are provided for each MMD,

[1] This document solely represents the views of the IEEE 802.3 Working Group, and does not necessarily represent a position of the IEEE, the IEEE Standards Association, or IEEE 802.

Transmit minimum, Transmit maximum, Receive minimum and Receive maximum. The sum of each value of each MMD provides the delay from the xMII, the timing reference point, to the MDI. This is illustrated in Figure 1 below.

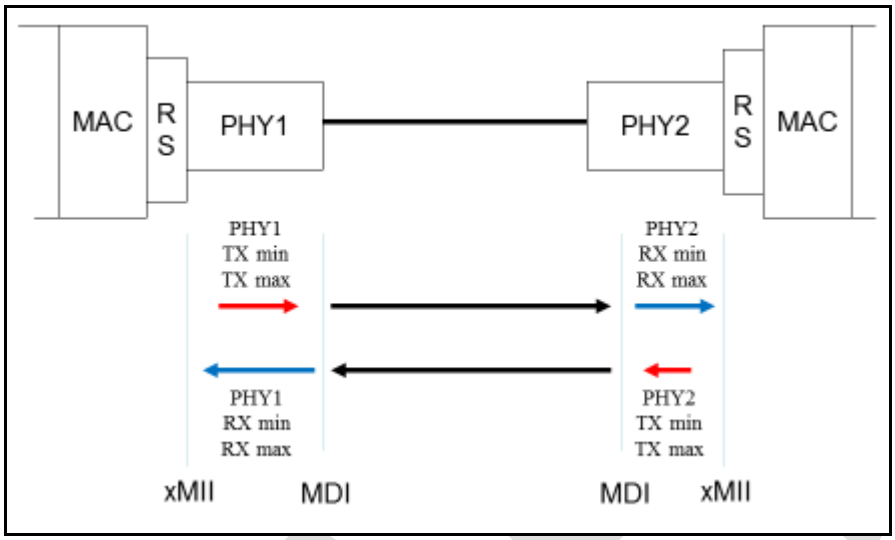

Figure 1

The difference between the maximum and minimum delays is due to path delay variability, for example due to crossing clock boundaries, and as noted in your liaison letter any variability impacts timing accuracy. An implementer is free to reduce these to the minimum possible to support high accuracy timing application. In addition the register values are valid when the link is established, and therefore can change values each time the link is established. This can be used to compensate for link start-up variations that will remain constant during link operation, for example FIFO depths.

The reference point used for the receive path data delay registers is the input of the beginning of the SFD at the MDI, however as noted in your liaison letter multi-lane PHYs may have different media lane delays resulting in differing arrival times for each lane. As illustrated in Figure 1 of your liaison letter the PCS lane deskew function (e.g., IEEE Std 802.3-2012 subclause 82.2.12) compensates for these different media lane delays by removing inter-lane skew. After removal of the inter-lane skew, the maximum skew variation at the output of the PCS lane deskew function for 40GBASE-R and 100GBASE-R is 4 ns (see IEEE Std 802.3-2012 Table 82-5).

Without a definition of which lane of the MDI is used as the timing reference point, as noted in your liaison letter, the entire inter-lane skew may need to be accounted for in the receive minimum and receive maximum path data delay register values. This is illustrated in Figure 2 below.

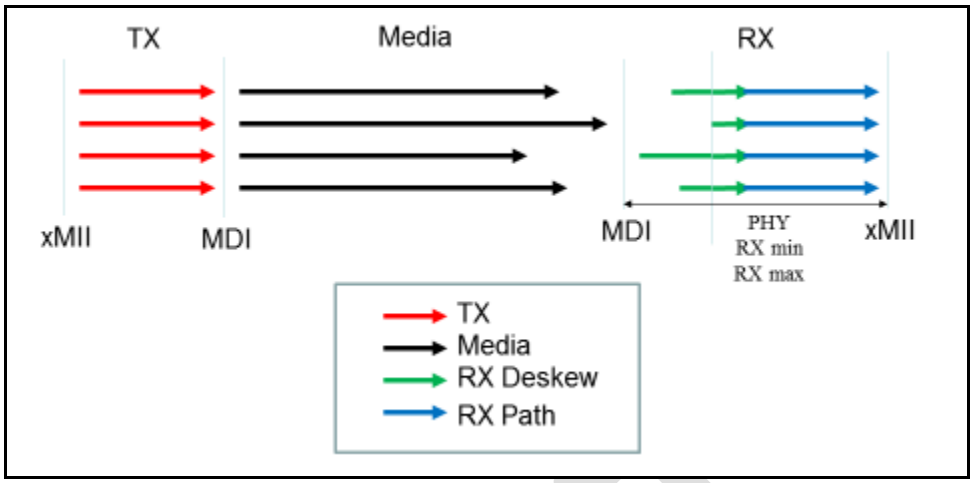

Figure 2

It is therefore suggested that the arrival of the SFD on the slowest lane of the MDI be used as the receive path reference point. This will have the effect of associating the alignment delay in excess of the slowest lane on the other lanes to the media, and reducing the delay uncertainly to that of the maximum skew variation. This is illustrated in Figure 3 below.

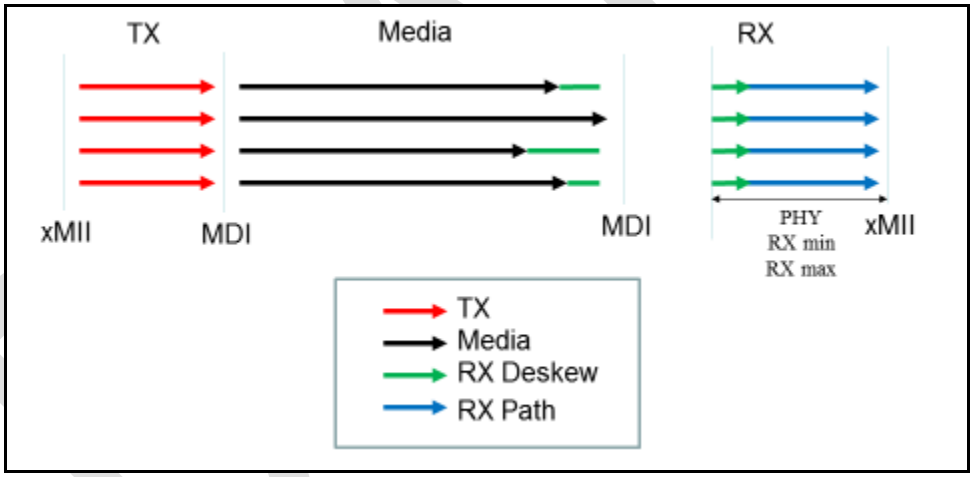

Figure 3

Please note that a maintenance request has been submitted to update IEEE Std 802.3 to use the arrival of the SFD on the slowest lane of the MDI as the timing reference point on multi-lane PHYs. This can be accessed at <http://www.ieee802.org/3/maint/requests/maint_1286.pdf>.

Sincerely,

David Law

Chair, IEEE 802.3 Ethernet Working Group