High Speed Token Ring PMD Options

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General Requirements

- *Must utilize existing PHY technology to meet time-to-market requirement*
- *Preferably standardized interface to MAC to utilize on-market components*
- *Preferably autosensing 4/16/High Speed*

Existing Technologies, Overview

- ***100Mbit Ethernet***
  - ***TX***
  - ***T4***
  - ***VG-AnyLAN***
- ***155Mbit ATM on UTP***
- ***100Mbit CDDI***
- ***Other possibilities?***
  - ***128Mbit - not generally available technology***

Ethernet 100Base-TX

- ***Full duplex capable, 125MHz over one pair in each direction, MLT-3 encoding***
- ***Requires two pairs UTP Cat. 5***
- ***Good backing, "has won" 100M Ethernet battle***
- ***Second generation silicon integrates PMD and PHY in single CMOS device***

- ***Integrated PHY/PMD support from at least***
  - ***Micro Linear***
  - ***ICS***
  - ***TDK Semi***
  - ***Level One***
  - ***More to follow (Intel, Davicom)***

Ethernet 100Base-T4

- ***Half duplex, 25MHz ternary data on three pairs (last pair for collision detect)***
- ***Requires 4 pairs UTP Cat. 3***
- ***Poor backing, more complex to design than anticipated***

- ***PHY/PMD support:***
  - ***Brooktree***
  - ***Cypress***
  - ***Pericom***

Ethernet 100VG-AnyLAN

- ***Half-duplex, transmits binary data on four pairs (demand priority, no collision detect)***
- ***Requires 4 pairs UTP Cat. 3***
- ***Loses backing, even from Hewlett-Packard***

- ***PHY/PMD support:***
  - ***Lucent Technologies***

ATM 155 UTP

- ***Full duplex, 155 MHz over one pair in each direction, MLT-3 encoding***
- ***Requires two pairs UTP Cat. 5***
- ***Current silicon requires multiple ICs: BiCMOS equalizer, serializer/deserializer with clock recovery***

- ***PMD equalizer support: GEC Plessey, Micro Linear, National, Pulse, TDK Semi, Wolfson and others***
- ***Related silicon support: AMCC, Fujitsu, IGT, PMC-Sierra, others***
- ***Silicon integration and migration to CMOS needed for cost effectiveness!***

FDDI over Copper

- ***Also known as: CDDI, SDDI and TP/FDDI***
- ***Full duplex capable, 100 MHZ over one pair in each direction, MLT-3 encoding***
- ***Requires two pairs UTP Cat. 5 or STP Type 1***

- ***PMD considerations as 100Base-TX***

Other Possibilities

- ***100Base-T2: 100Mb/s over one pair in each direction, Cat. 3 with CAP modulation***
- ***Emerging technology (not commercially available yet), expensive***

- ***ATM 155 over Cat. 3 with CAP modulation (Carrier-less Amplitude-Phase)***
- ***Emerging technology (not commercially available yet), expensive***

MAC Standard Interfaces

- ***MII (Media Independent Interface):***
  - ***Nibble-wide 25MHz full duplex data, dominant in 100 Ethernet***
  - ***Includes serial management path with well defined register set***
  - ***Includes dedicated control pins for Ethernet (both T and VG)***

- ***UTOPIA Level 1 (Universal Test and Operations PHY Inteface for ATM):***
  - ***Byte-wide 25MHz full duplex data, dominant in ATM 155***
  - ***No management path included***

- ***SATURN:***
  - ***Derivative of UTOPIA, used by PMC-Sierra (S/UNI-Lite)***
  - ***No management path included***
  - ***Both UTOPIA and SATURN control signals match to ATM cells only***

Conclusion, PMD

- ***PMD Recommendation:***
  - ***100Base-TX best choice for cost effectiveness and silicon availability***
  - ***ATM155 PMD is faster (could be “160/16”), but currently at double cost***

- ***PMD key functional blocks:***
  - ***Adaptive equalizer, Baseline Wander Correction, Clock recovery PLL, serializers can be all inherited directly from 100Base-TX***

Conclusion, PHY/MAC Interface

- ***PHY/MAC Interface:***
  - ***MII interface best choice to match 100Mbit/s with integrated management path***
  - ***Existing devices are not directly suited for High Speed Token Ring: No need for 4B5B encoder, scrambler, auto-negotiation***

  - ***Standard management registers must be defined (like MII)***
  - ***Standard need only define High Speed part, dual speed support is left to individual implementation***