100 Mbit/s 802.5 PHY Layer – 100BaseTX Review

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A Quick Review of the MII (Media-Independant Interface)

- Exposed interface is NOT required
- Standardized connector and signal levels if exposed

1. Transmit Data

A. TXD<3:0> (Transmit Data) Nibble wide data line
B. TX_EN: (Transmit Enable) "Framing" Signal – generates special two-nibble data words at both assertion and de-assertion
C. TX_ER: (Transmit Error) Signal to Reciever that transmit data is bad.
D. TX_CLK: (Transmit Clock) Generated by the PHY, synchronizes data flow

2. Receive Data

A. RXD<3:0> (Receive Data) Nibble wide data line
B. RX_DV: (Receivd Data Valid) "Framing" Signal – strips special two-nibble data word
C. RX_ER: (Receive Error) Asserted when "invalid" code is received
D. RX_CLK: (Receive Clock) Generated by the PHY, synchronizes data flow

3. Signaling

A. CRS: (Carrier Sense) Asserted when non-idles are received
B. COL: (Collision) Asserted when Transmitting Frame (TX_EN high) AND receiving carrier. Not used in Full duplex

Not Required to be synchronous with RX_CLK or TX_CLK

4. Station Management

A. MDIO: (Management Data Input/Output) Bidirectional serial data line
B. (Management Data Clock) gnerated by the MAC

- Always initiated by the MAC

- Two “Basic” and seven optional “Extended” 16 bit registers with pre-defined bit interpretations.

A Quick Review of the TX Transmission

- 4B/5B encoding
- Nibble synchronization occurs ONLY when “JK” – special code word associated with start of frame – is received.
- Scrambling occurs after 4B/5B *(type/size of scrambler)*
- MLT-3 Transmitted signals
- UTP and STP interface definitions
- 2Vp-p, 5% overshoot, 4ns rise time, 0.5ns DCD, 1.4 ns jitter
- Optional Far End fault detect

A Quick Review of Auto-Negotiation

- Signalling via bursts of 10BaseT Link Test Pulses, called a Fast Link Pulse (FLP) burst.
- Odd FLPs generate clock.
- Presence or absence of even FLPs encode data bits.
- Both PHYs transmit “abilities” repeated.
- Priority of negotiation is pre-determined.
- TX signalling initiated when negotiation is determined.
- TX synchronization required for completion signal.
- Completion signalled through serial management, failure is NOT reported.
- 8 bits on base page plus 11 bits each on multiple “next” pages
- Detection of 100BaseTX data performed in parallel.

AN Parallel Detection

- Prior to start of AN, and between retries of AN perform “parallel detect”
- PMA detects if own protocol is present on cable
- If detects good signal, then AN completes and Link_Status is asserted
- AN may be disabled with bit 0.9 of Control Reg.
- 802.3 is FORCING AN capability (not allowing parallel detect) on new protocols, e.g. 100BaseT2.

Auto-Negotiation: The Full Story

⇒ Assumption #1: Selector field set to 802.5 because 802.3 setting will not be acceptable to standards body.

⇒ Assumption #2: Auto-Negotiation should work with existing TX implementations.

- Multiple existing PHYs support writable advertised-ability fields. Few support next page capability.
- There is no standard (certain) procedure to determine when the partner-ability field is correct – no registers are guaranteed to be valid until A-N is successfull, and A-N will never be successfull with 802.5 selector.
- Procedure may still work in existing TX implementations compare values in link partner ability reg. to advertised ability reg. and not to the hard-wired 802.3 value.
  - ◊ In this case, the 802.5 register definitions must map such that the negotiation settles on Full Duplex 100BaseTX protocol.
  - ◊ Priorities:

1) TX Full Duplex
2) T4
3) TX
4) 10BaseT Full Duplex
5) 10BaseT

Issues

1) Support Auto-Negotiation vs. Parallel Detect Only
2) Fix 802.3 PHY date&version vs. Track future changes
3) Use Link_Status bit vs. Timer to start registration
4) Standardize rate auto-detect vs. Ignore issue in standard