Investigating the effects of relaxing the return loss specifications from those given in TP-PMD.

Introduction.

These notes present the results of an investigation into the effects - particularly on long cable length performance - of relaxing the return loss specifications from those given in TP-PMD, i.e. as described in ANF-06 and ANF-07.

The investigation covers two main areas.

The first is the contribution to the degradation in eye opening at an HSTR receiver due to reflections arising from the use of a 'compromise' transceiver impedance match in place of discrete 100Ω and 150Ω impedances for UTP and STP respectively. A simplified transceiver and cable together with a representative isolation transformer circuit is modelled in PSpice and the results of practical testing are presented.

The second is a comparison of the effects of a compromise match in the presence of stray capacitance typically encountered due to PCB layout and device capacitances. The effects of stray capacitance with a pure resistive load are compared with those obtained by a transformer coupled resistive load (with the same representative transformer model as used in the jitter modelling).

Jitter investigation.

The notes are split into two sections, the first covering PSpice simulation work and the second covering practical work.

PSpice simulation work.

A simplified transceiver model was simulated in PSpice using a differential voltage source in series with a real source resistance, which is connected to the Phy side of a representative transformer model of 1:1 turns ratio. The line side of the transformer is connected via a lossless transmission line of 27ns length, with a real (resistive) impedance, to a real load resistance.

A capacitance of 8pF is placed in parallel with the source resistance at the Phy side connections of the transformer to represent stray capacitance, in addition to that included in the transformer model itself.

The voltage source was set up to generate an arbitrary MLT-3 signalling sequence of 220 bits in length.

This model specifically neglects the contributions to jitter that are independent of transceiver matching impedances. Therefore, contributions due to mismatches between horizontal cabling and patch cord segments, NEXT and the frequency dependant effects of cable attenuation are not modelled.

Six versions of this model were simulated.

1. A 2V pk-pk open circuit voltage 100Ω source with an 85Ω transmission line into a 100Ω load. This provides a reference eye diagram for a discrete 100Ω match at the lower impedance extreme of UTP.
2. A 2.45V pk-pk open circuit voltage 150Ω source with a 165Ω transmission line into a 150Ω load. This provides a reference eye diagram for a discrete 150Ω match at the upper impedance extreme of STP.
3. A 2.45V pk-pk open circuit voltage 124Ω source with an 85Ω transmission line into a 124Ω load. This provides an eye diagram for a compromise 124Ω match at the lower impedance extreme of UTP.
4. A 2.45V pk-pk open circuit voltage 124Ω source with a 165Ω transmission line into a 124Ω load. This provides an eye diagram for a compromise 124Ω match at the lower impedance extreme of STP.
5. A 2.45V pk-pk open circuit voltage 124Ω source with an 85Ω transmission line into a 100Ω load.

This provides an eye diagram for a compromise transmit 124Ω match into a discrete 100Ω receive match with a cable at the lower impedance extreme of UTP.

6. A 2.45V pk-pk open circuit voltage 124Ω source with a 165Ω transmission line into a 150Ω load. This provides an eye diagram for a compromise transmit 124Ω match into a discrete 150Ω receive match with a cable at the upper impedance extreme of STP.

A compromise match of 124Ω was used because (a) this is close to the ideal impedance of 122.5Ω when attempting to achieve the best return loss at both 100Ω and 150Ω as is being proposed for the HSTR standard, and (b) this represents the worst departure from a true 100Ω match - when considering operation over UTP - at which testing has currently been carried out.

The transmission line of the model was then changed to a series connection of three lossless lines comprising a 5ns line of 85Ω, a 13ns line of 115Ω and a 9ns line of 85Ω.

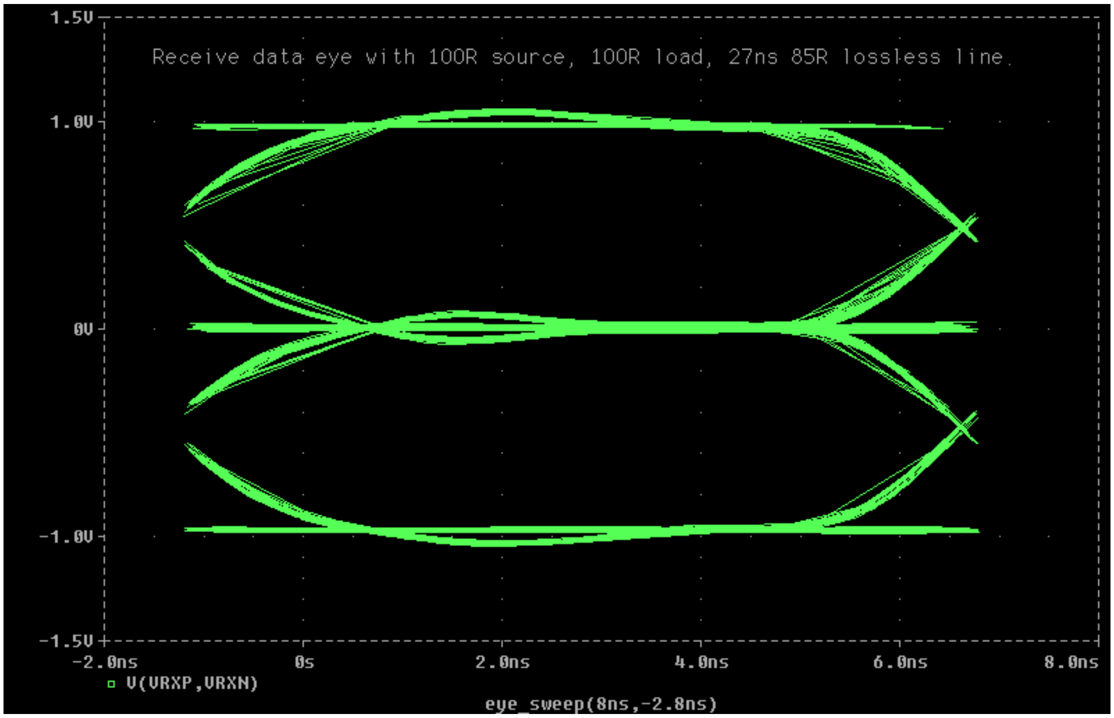
This represents two lengths of UTP patch cord and a length of rigid UTP at their impedance extremes.

Two further versions of this model were then simulated;

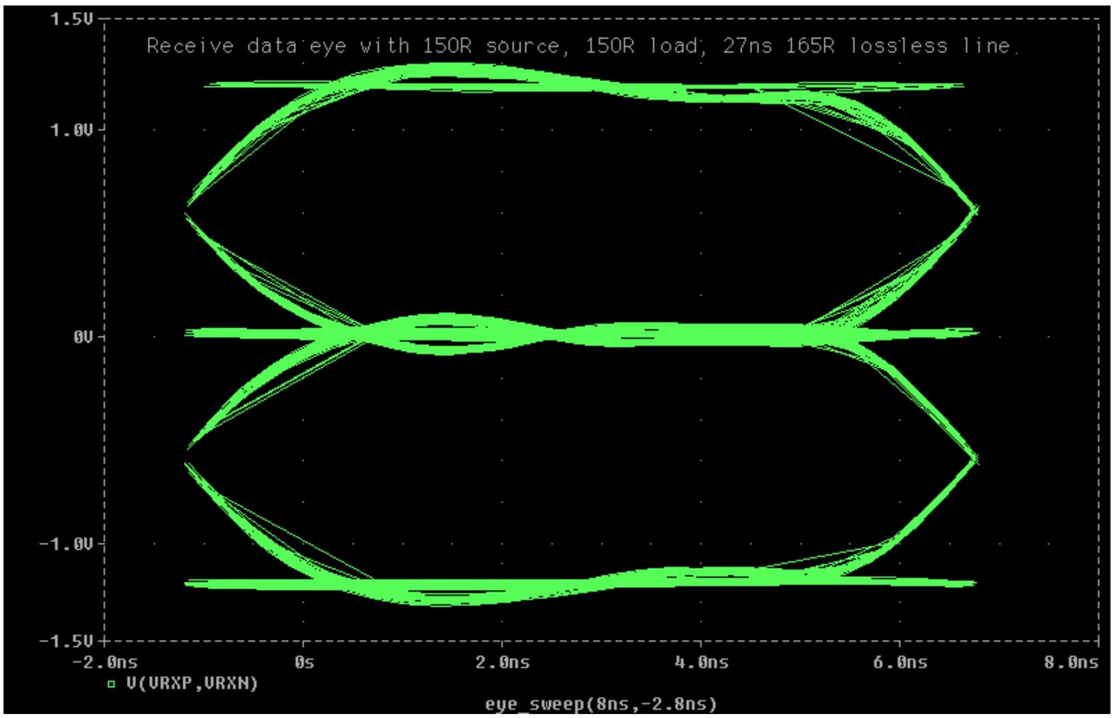
7. A 2V pk-pk open circuit voltage 100Ω source with the three transmission lines into a 100Ω load.
8. A 2.45V pk-pk open circuit voltage 124Ω source with the three transmission lines into a 124Ω load.

Jitter simulation results.

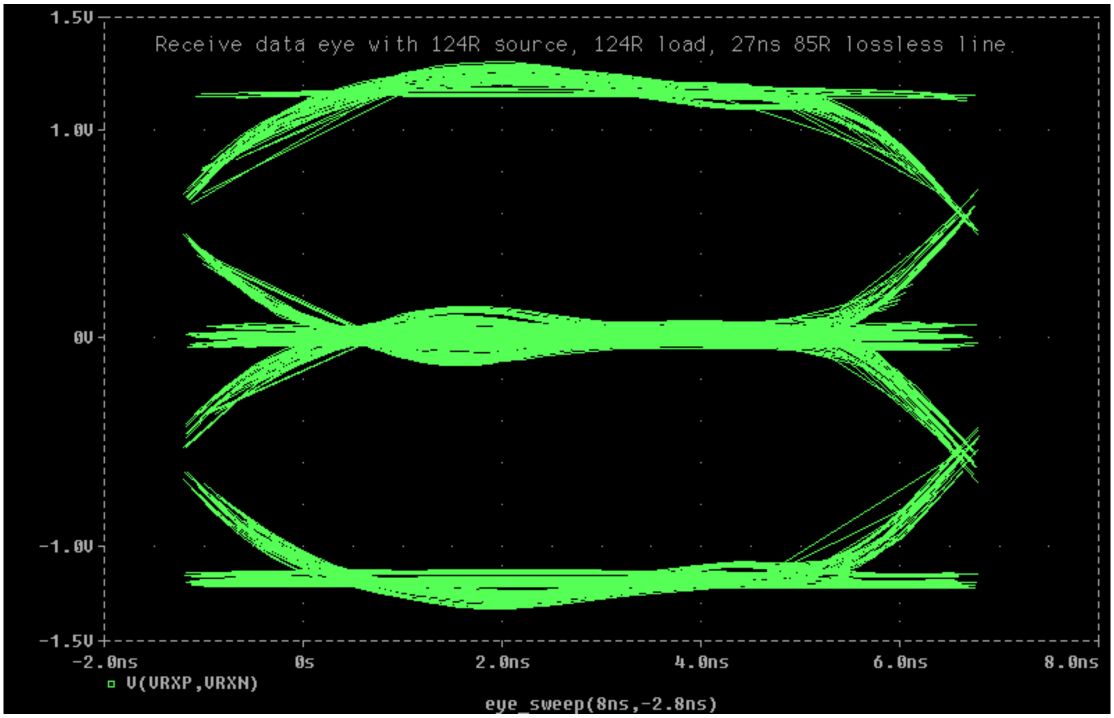
The results of these 8 simulations are shown below.



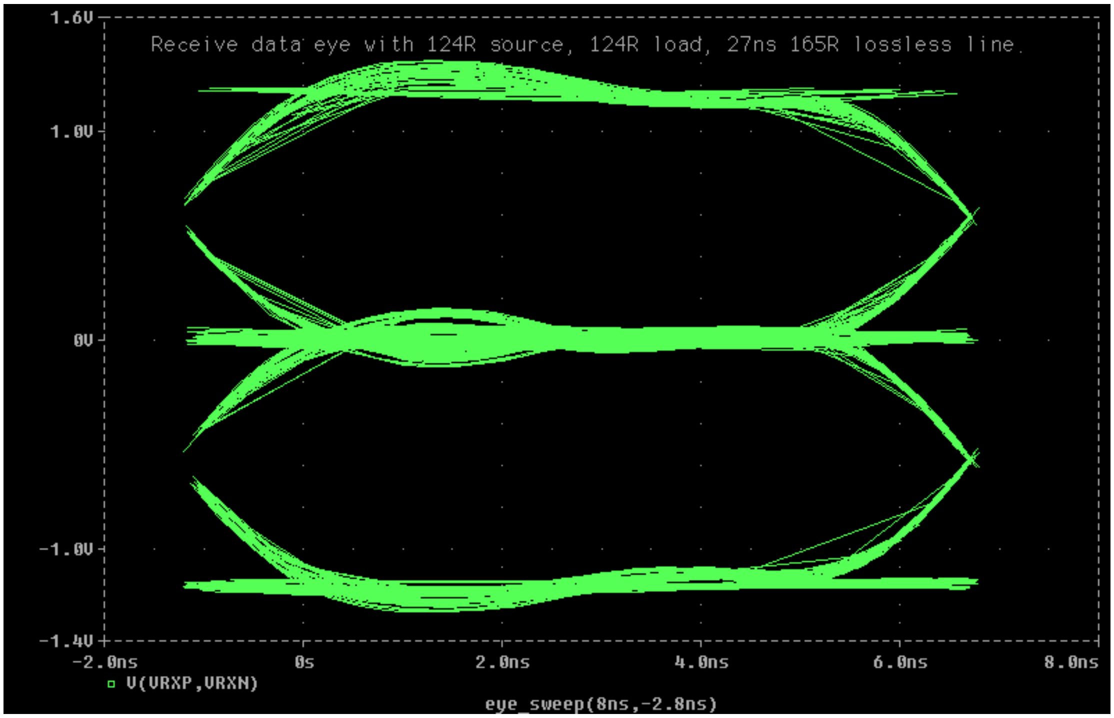
Simulation 1



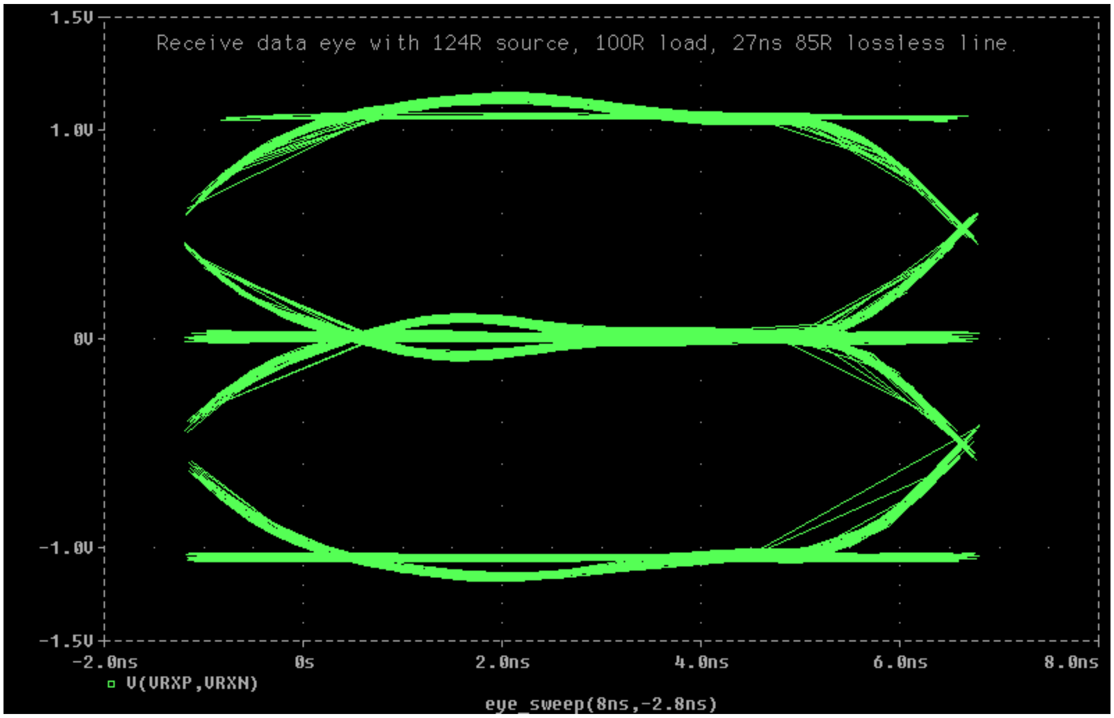
Simulation 2



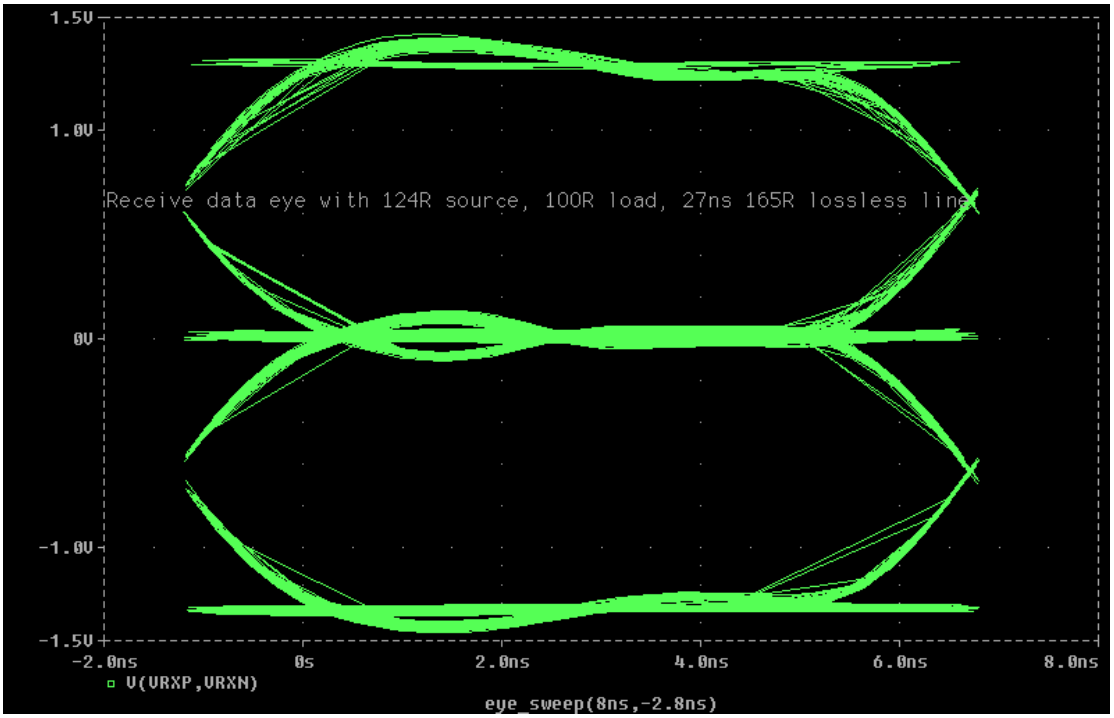
Simulation 3



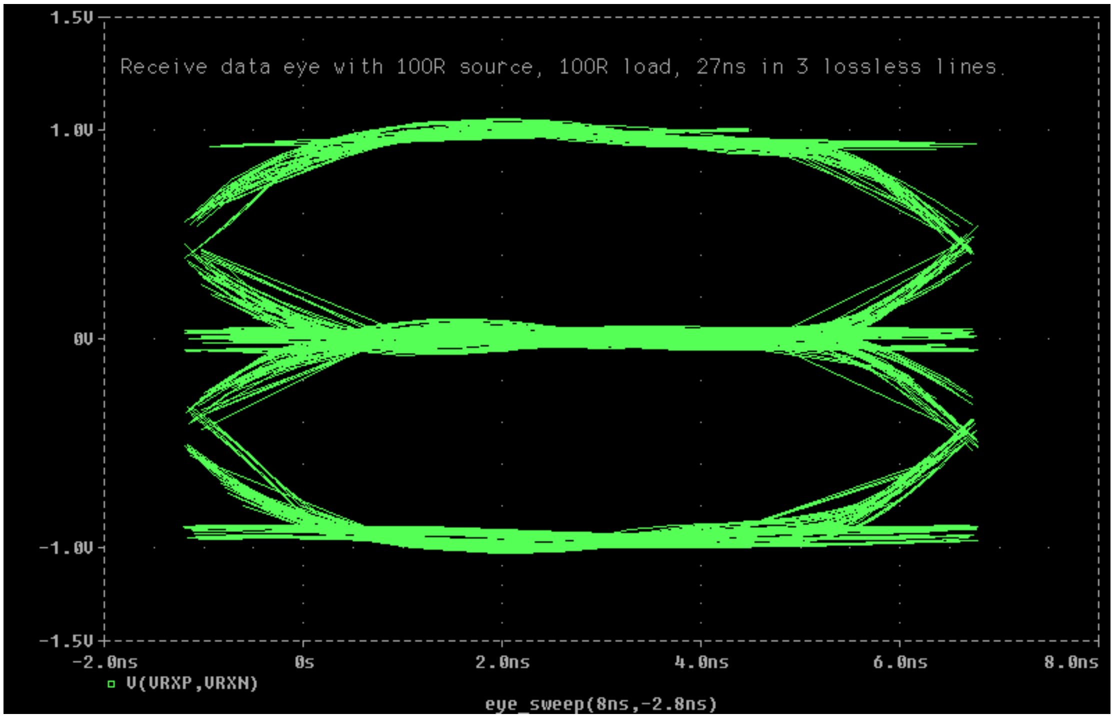
Simulation 4



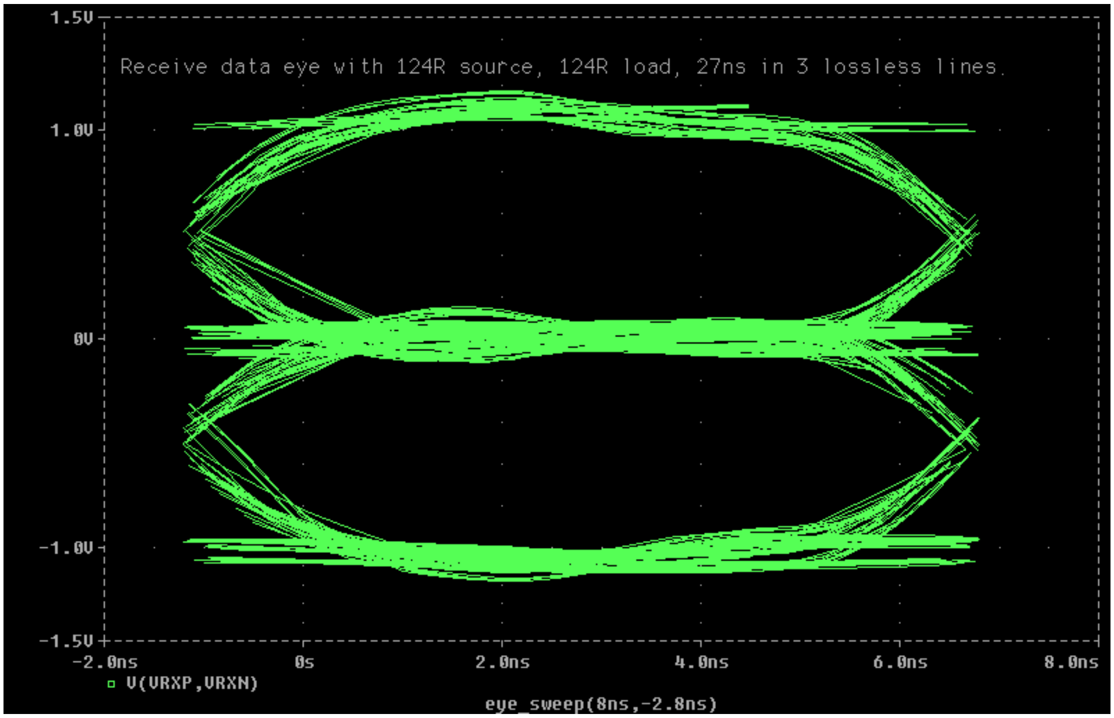
Simulation 5



Simulation 6



Simulation 7



Simulation 8

Simulations 1 – 6 show that there is only slight degradation in eye opening due to using a compromise match of 124Ω instead of the discrete values of 100Ω or 150Ω.

Simulations 7 & 8 show that for UTP cabling there is greater degradation in eye opening due to the possible mismatch between cable segments than due to using a compromise match of 124Ω instead of the discrete values of 100Ω or 150Ω.

Practical testing.

Testing was carried out by setting up links with the same matching impedance at each end, for 100 ohms, 118 ohms and 124 ohms. A test sequence comprising 200 sets of 1000 off 512 byte frames.were sent over the link with each impedance; first with a set of UTP and then again with a set of STP cable segments. In each case the cable lengths were reduced by swapping segments in and out zero errors were obtained over repeated runs.

The cabling was set up as described below.

UTP;

(9m+7m) Cat5 patch + 100m Cat5 rigid + [(A+B) or (B+C) or (A+C)] Cat5 patch

> where;
> A = 9m, B = 7m and C =5m.

This means that linear distances of 128m, 130m and 132m could be set up.

Segments were joined using cheap RJ45 back to back connectors that are definately *not* Cat5.

This was to try to set up a reasonably representative cabling example.

STP;

0.5m RJ45 to DB9 STP patch + [X] + 3m DB9 to MIC_S patch + 150m MIC_S TYPE1 cable + 100m MIC_S TYPE1 cable + [Y] + 3m DB9 to MIC_S patch + [X] + 0.5m RJ45 to DB9 STP patch

> where;
> [X] means zero or 3m DB9 to DB9 patch
>
> and
> [Y] = 10m or 20m MIC_S TYPE1 cable.

This means that linear distances of 267m, 273m, 277m or 283m could be set up.

This was to try to set up a reasonably representative cabling example.

Practical testing results.

The results obtained were;

UTP;

100 ohms: 128m
118 ohms: 128m
124 ohms: 128m

STP;

100 ohms: 267m
118 ohms: 273m
124 ohms: 277m

For both cable types, similar figures were also obtained for cases where source and destination impedances were not equal.

Return loss investigation.

PSpice simulation work.

This work follows on from the work presented in Bo Thomsens paper 07-19.

Figure 1 below shows how the return loss from an 85Ω source into a pure resistive 100Ω termination varies with parallel capacitance

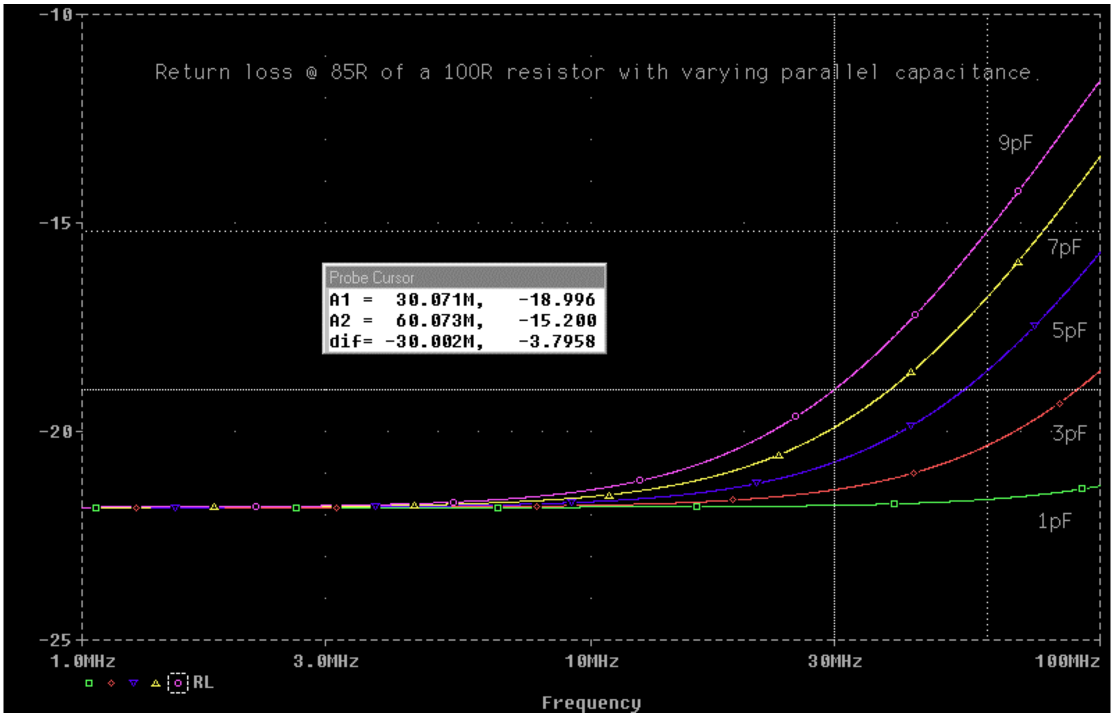


Figure 1.

Figure 2 below shows how the return loss from an 165Ω source into a pure resistive 150Ω termination varies with parallel capacitance.

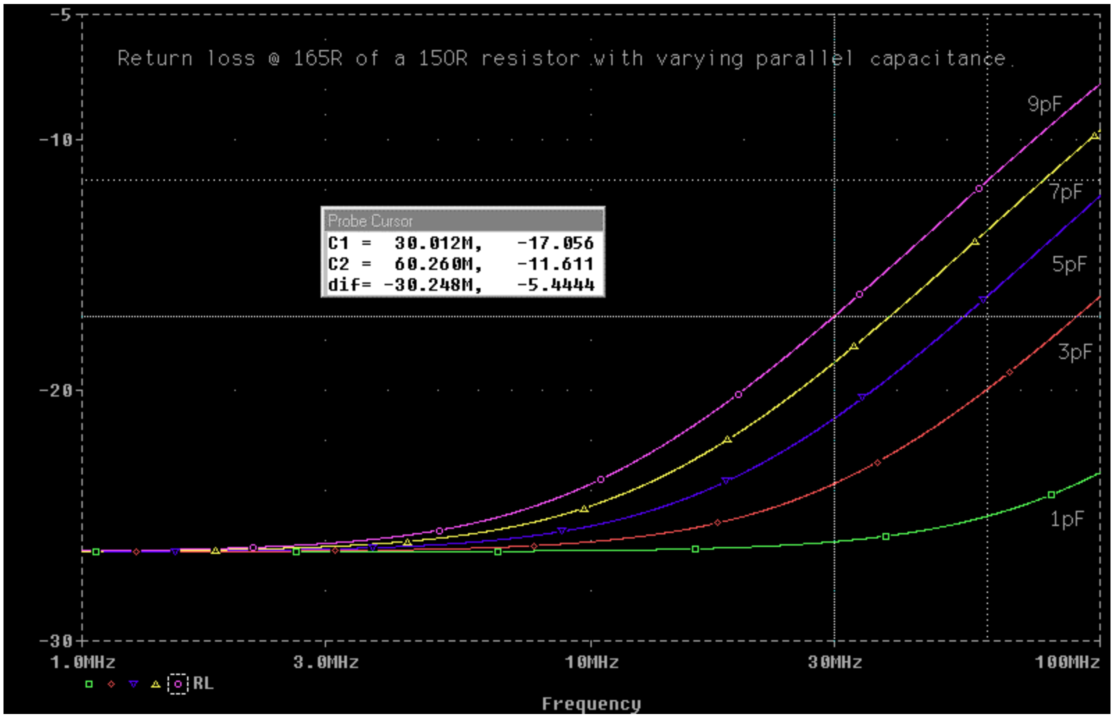


Figure 2.

Figure 3 below shows how the return loss from an 85Ω source into a pure resistive 124Ω termination varies with parallel capacitance.

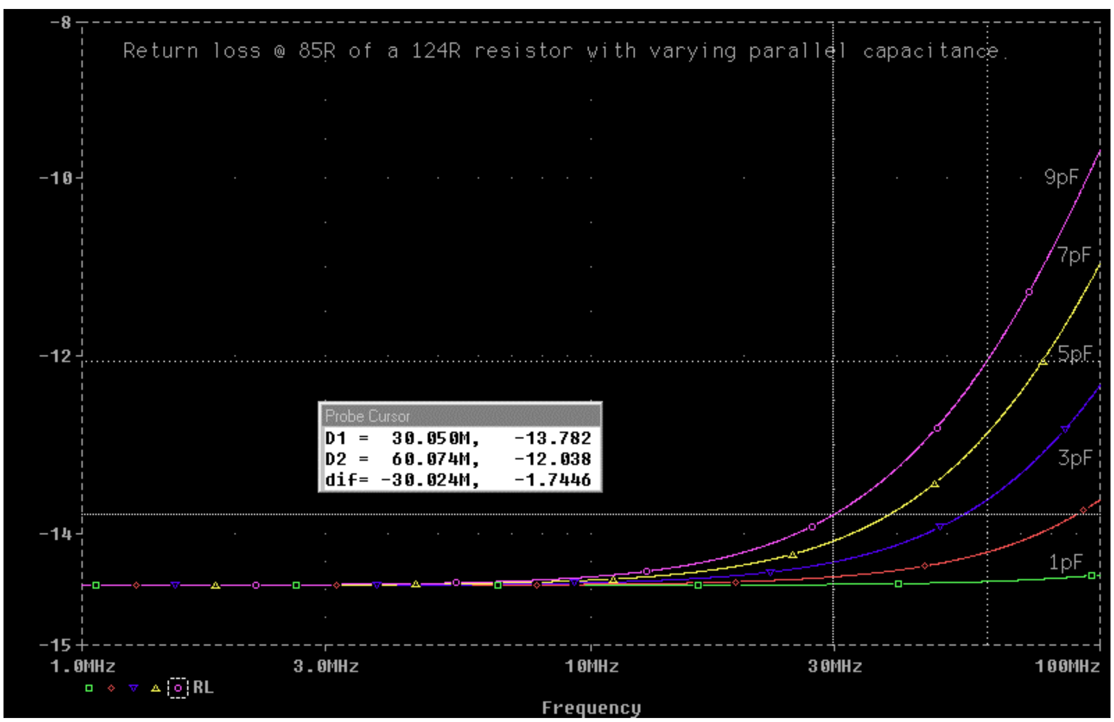


Figure 3.

Figure 4 below shows how the return loss from a 165Ω source into a pure resistive 124Ω termination varies with parallel capacitance.

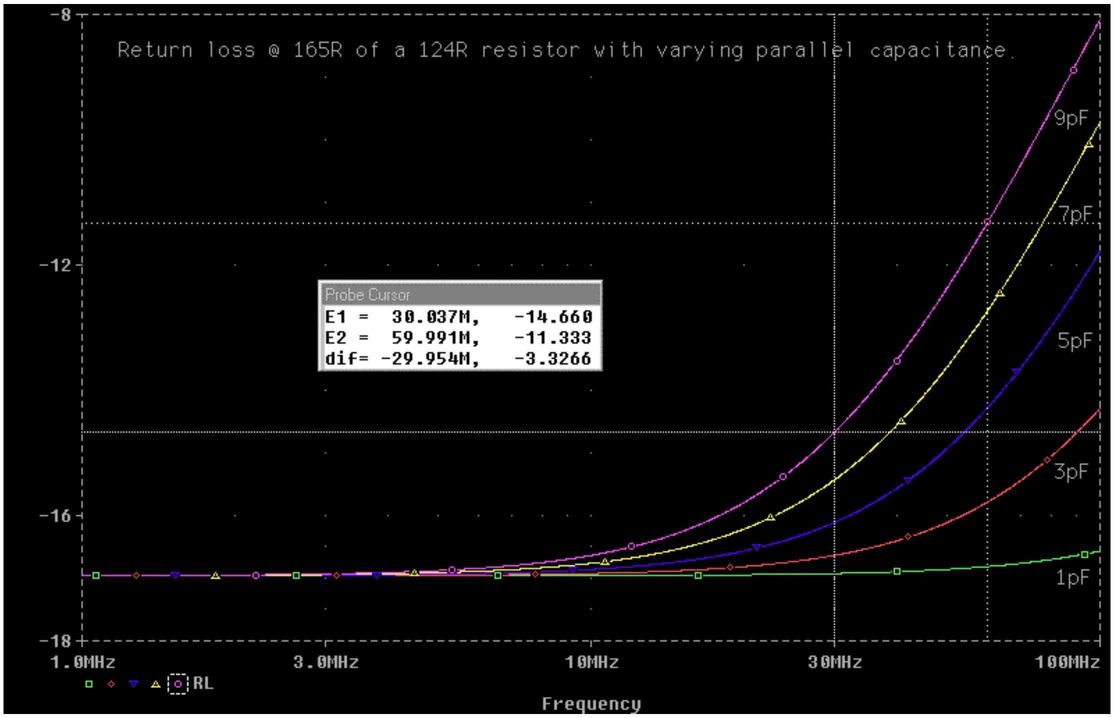


Figure 4.

These results are basically the same as those presented in 07-19. However, the introduction of a transformer markedly changes the situation.

Figure 5 below shows how the return loss from an 85Ω source into a transformer coupled pure resistive 124Ω termination varies with parallel capacitance.

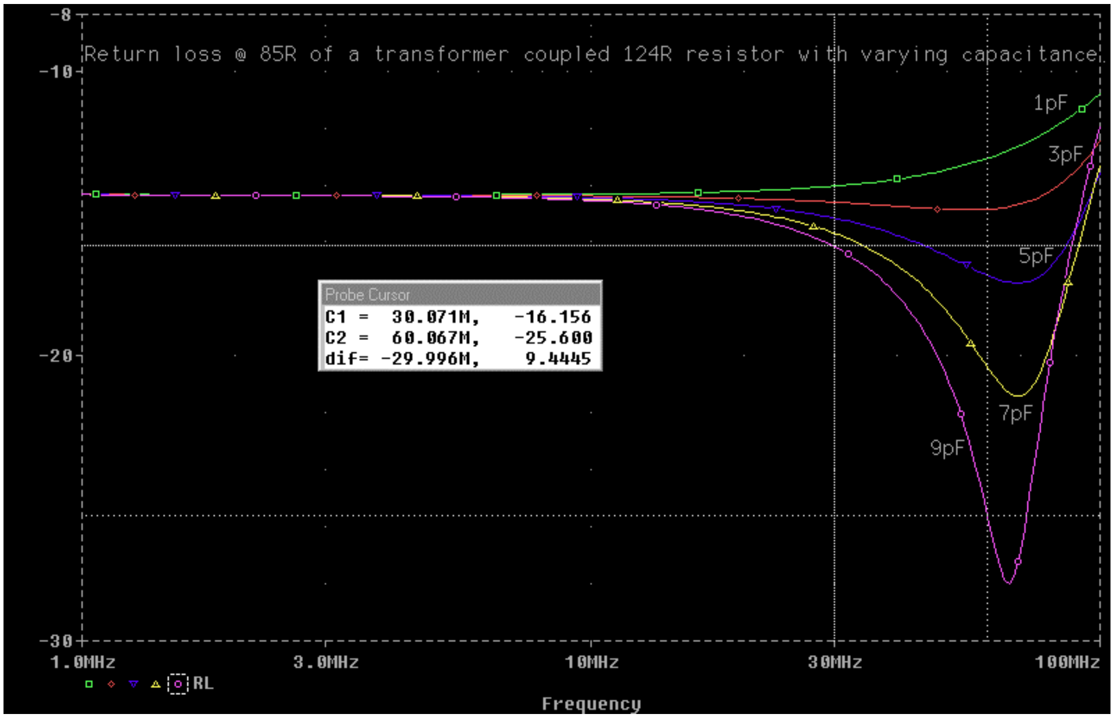


Figure 5.

Figure 6 below shows how the return loss from a 165Ω source into a transformer coupled pure resistive 124Ω termination varies with parallel capacitance.

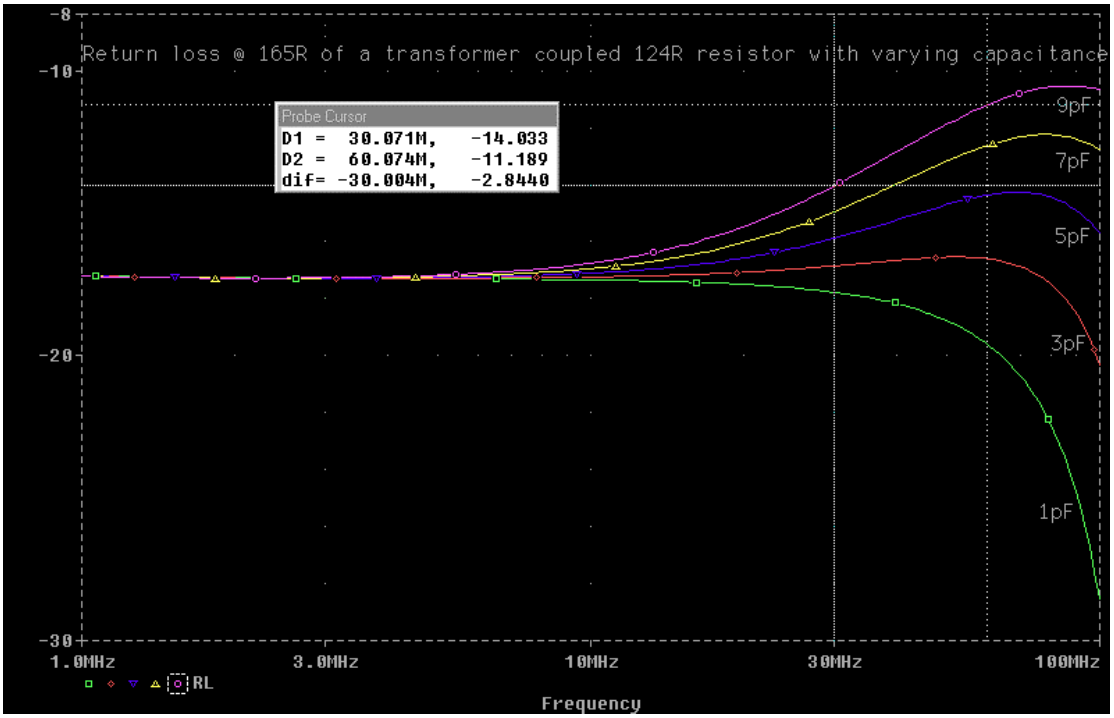


Figure 6.

It is important to note that the effect of the stray capacitance is inverted between the UTP and STP cases of Figures 5 and 6. From these two figures it can be seen that a capacitance of approximately 3pF with this transformer model would give a substantially flat return loss of about 14dB for UTP and 16dB for UTP.

To try to gain a little more insight into this behaviour, Figures 7 & 8 show the effect of varying the termination resistance for a given load capacitance.in both UTP and STP cases.

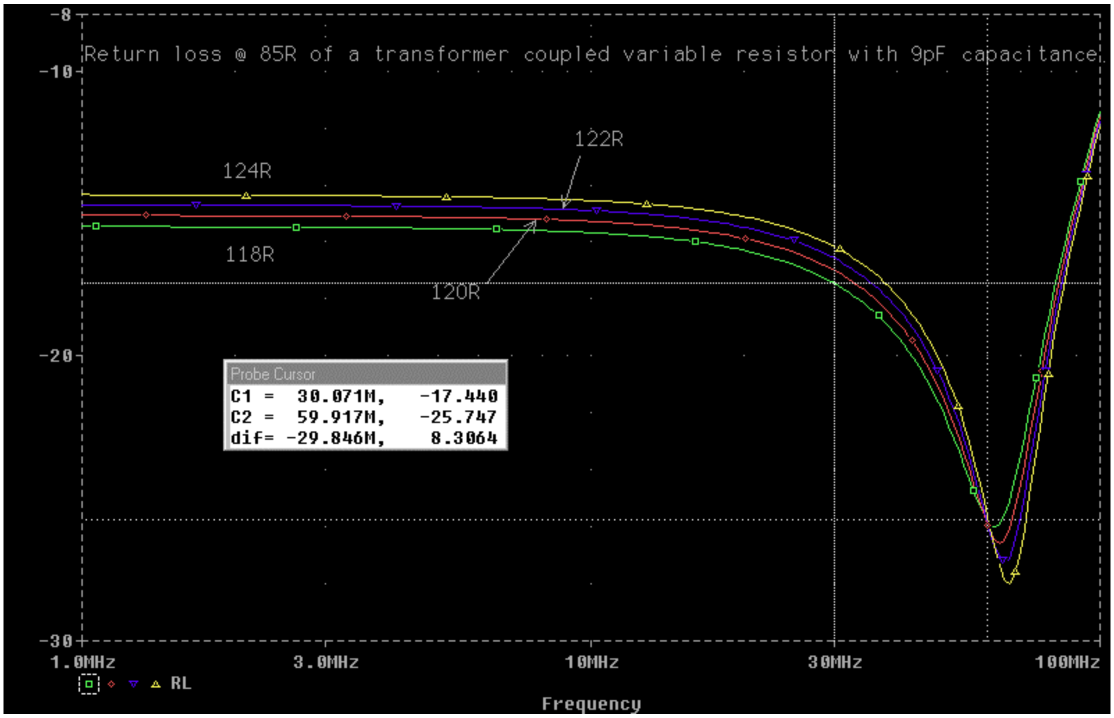


Figure 7.

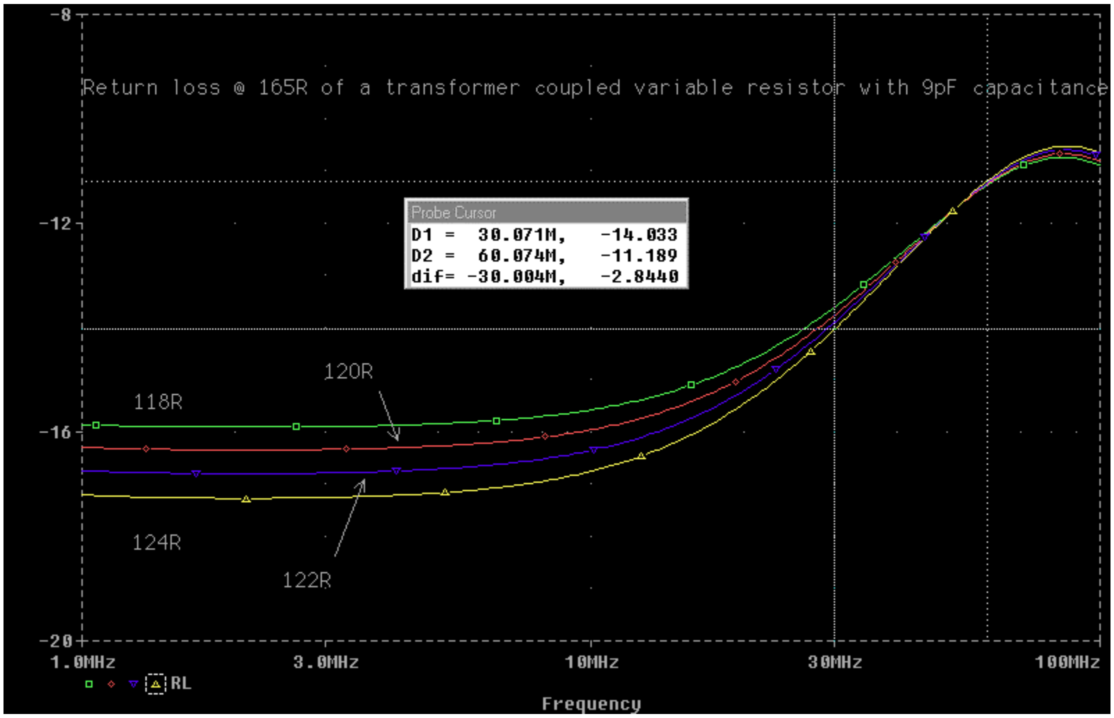


Figure 8.

Note in these two figures that the high frequency return loss is dominated by the transformer parameters and circuit capacitances due to layout and Phy device parameters, rather than directly by the termination resistance. This effect continues to hold even for ideal 100Ω UTP matching and 150Ω STP matching.

Conclusions

It is worth noting that the situation being investigated here is not the same as that which was investigated some years ago with regard to the support of 120Ω cabling. In that case the major jitter contribution arose due to the 100Ω or 150Ω cable to 120Ω cable mismatches, which the results shown here indicate would be considerably worse again than those shown for Simulation 7.

Experimental results have shown that operation with 128m of mixed UTP cabling, and 270m of mixed STP cabling can be achieved with this compromise match. Although no tests have been done for a pure 150Ω match, it is expected that the increase that this would make to the STP operational length would be in the region of 10m - 20m. It was also found that, with a 124Ω match, an operational length of 150m could be achieved on a less ‘difficult’ cabling setup comprising only two lengths of Cat5 solid core UTP, whilst an accidental set up actually gave a reliable connection - albeit with degraded error performance - over a 200m single run of Cat5 UTP patch cable.

From the figures shown above illustrating return loss behaviour with overall termination impedance, it can be seen here that the high frequency return loss is dominated by the transformer parameters and circuit capacitances due to layout and Phy device parameters, rather than directly by the termination resistance. Since the transformer parameters and circuit capacitances tend to be the dominant components in a real implementation it is not too surprising therefore that cable length performance is fairly insensitive to matching impedance.

From this study, the experimental results that have been obtained and from discussions with a number of other implementors, the overall conclusion is that the use of a ‘compromise’ matching impedance causes negligible reduction in the achievable operational length over UTP and causes no significant reduction in achievable operational length over STP.