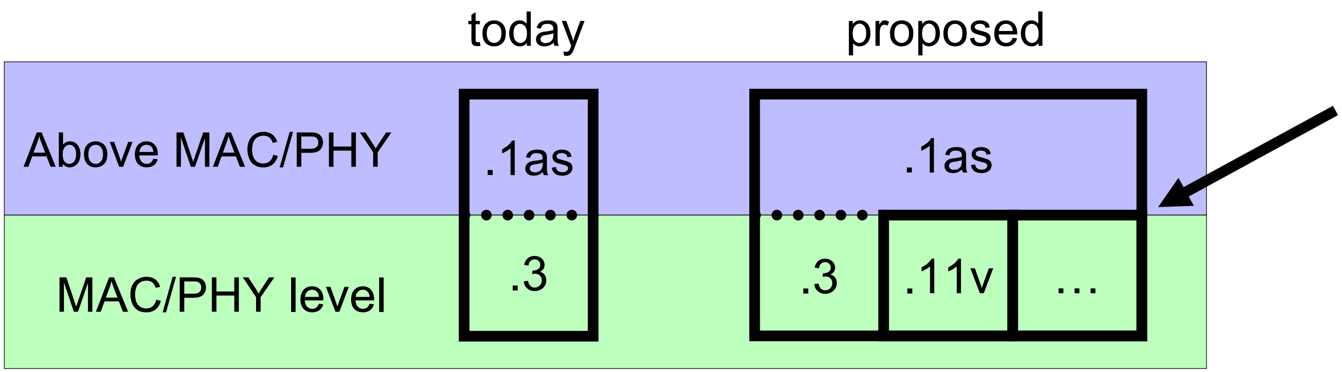
AV Time Synchronization Model

Dirceu Cavendish
NEC Labs

GOALS



802.1as will extend the service interface with timestamp. We must ensure the extension is generic enough to work for .11

- Define interoperability features
  - Bridging “Time” from one LAN to another
    - Interoperation between LANs
  - Define extension to MAC Service Interface to get timestamps
- Measurement:
  - Define timestamp snapshot precisely across various PHYs (.3, .11)
  - Define measurement accuracy options
- Protocol:
  - Define “Generic Messages” example
    - Would be used for 802.3 networks
  - Non 802.3 media would use the “Generic Messages” or define their own

802.3 architecture and timestamps

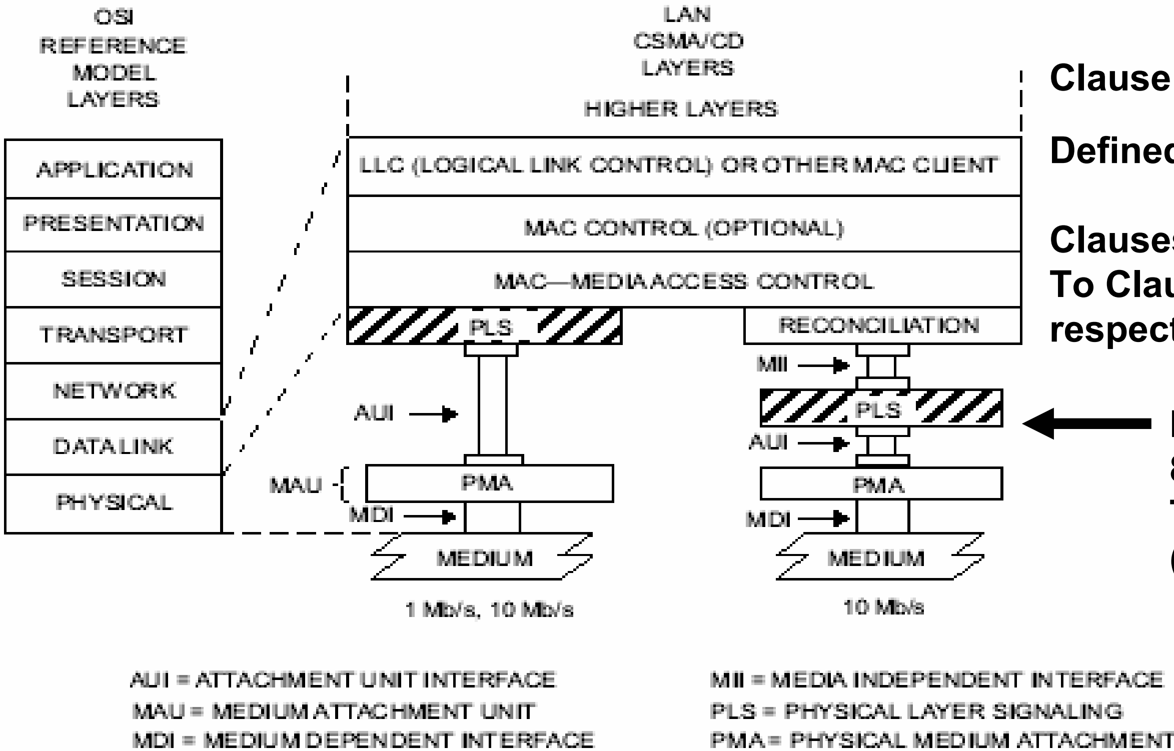


Figure 6–1—PLS service specification relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and the IEEE 802.3 CSMA/CD LAN model

Clause 6 – Physical Signalling Service

Defined for 10Mb/s speeds

Clauses 22, 35, and 46 define mappings To Clause 6 for 100Mb/s, 1Gb/s, and 10Gb/s, respectively

Delay tolerance
802.3-2005
Table 35-5 GMII
(48bits from TX_EN)

MAC PLS service
(Std 802.3-2005 6 – 10Mb/s)

PLS_DATA.request (OUTPUT_UNIT) [6.3.1.1.2] : MAC request to transmit a single data bit.
OUTPUT_UNIT can have values of ONE, ZERO, or DATA_COMPLETE

PLS_DATA.indication (INPUT_UNIT) [6.3.1.2.2]: Generated to all MAC sublayers after a PLS_DATA.request is issued.
INPUT_UNIT can have ONE or ZERO values.

ISSUES:
-Not clear what a PLS data_unit is – 802.3 frame/bit?
BIT
-Not clear when PLS_DATA.indicate is issued as related to an incoming data/frame.
PLS_CATA.indicate is generated for each bit received.

Proposal for Time/sync in 802.3 architecture

GMII Reconciliation sublayer (Std 802.3-2005 35.2.1)

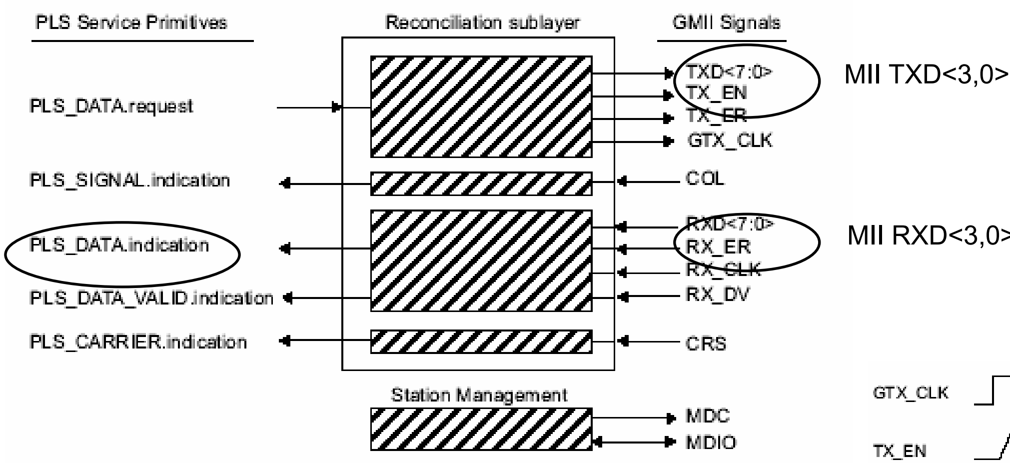


Figure 35–2—Reconciliation Sublayer (RS) inputs and outputs and STA connections to GMII

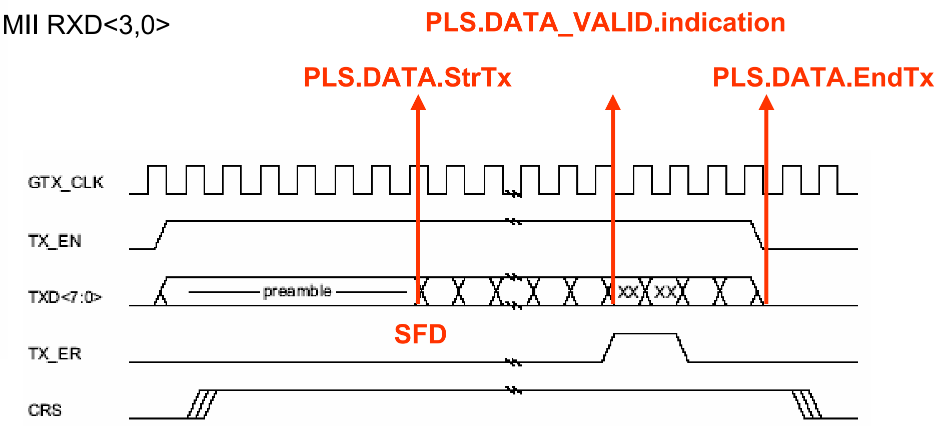


Figure 35–4—Propagating an error within a frame

MAC PLS service (Std 802.3-2005 35 – 1Gb/s)

PLS_DATA.request (OUTPUT_UNIT) [35.2.1.1.2] : MAC request to transmit a single data bit.
OUTPUT_UNIT allowed values: ONE, ZERO, TRANSMIT_COMPLETE, EXTEND, EXTEND_ERROR

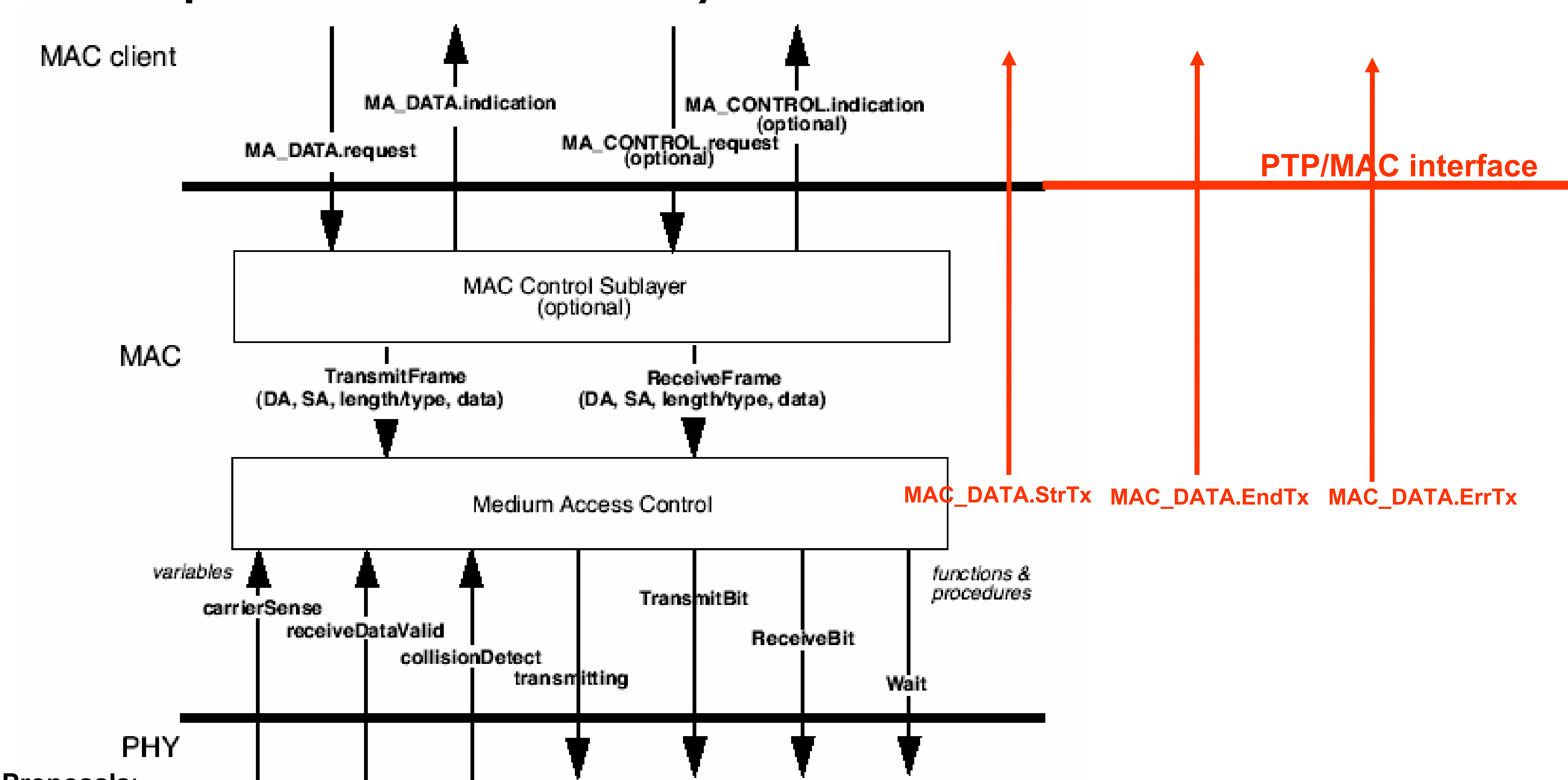
PLS_DATA.indication (INPUT_UNIT) [35.2.1.2.2]: Generated to all MAC sublayers after a PLS_DATA request is issued.
INPUT_UNIT allowed values: ONE, ZERO, EXTEND.

PLS_DATA_VALID.indication (DATA_VALID_STATUS) [35.2.1.7]: Generated when DATA_VALID_STATUS change occurs.
DATA_VALID_STATUS allowed values: DATA_VALID, DATA_NOT_VALID.

PLS_DATA.StrTx: marking beginning of transmission on PHY.

PLS_DATA.EndTx: marking end of successful transmission on PHY.

Proposal for Time/sync in 802.3 architecture



Proposals:

1 – RS supports additional timing signals

-MAC client implements PTP protocol

-Timestamp handled at PTP (LLC) sublayer.

-MAC sublayer needs to generate MAC_DATA.StTx, MAC_DATA.EndTx, MAC_DATA.ErrTx

-MAC sublayer needs to receive PLS_DATA.StrTx and PLS_Data.EndTx

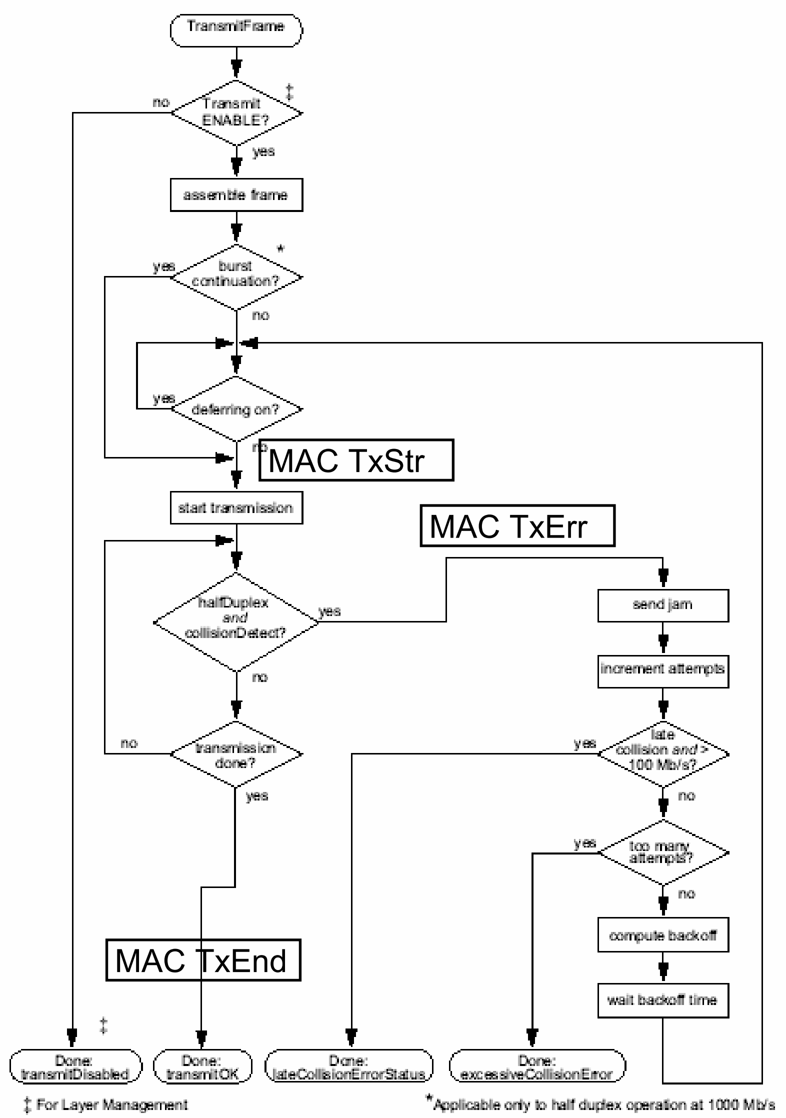
-Issues:

-Preamble shrinkage – SFD jitter

-TX and RX clock mismatch – SFD jitter

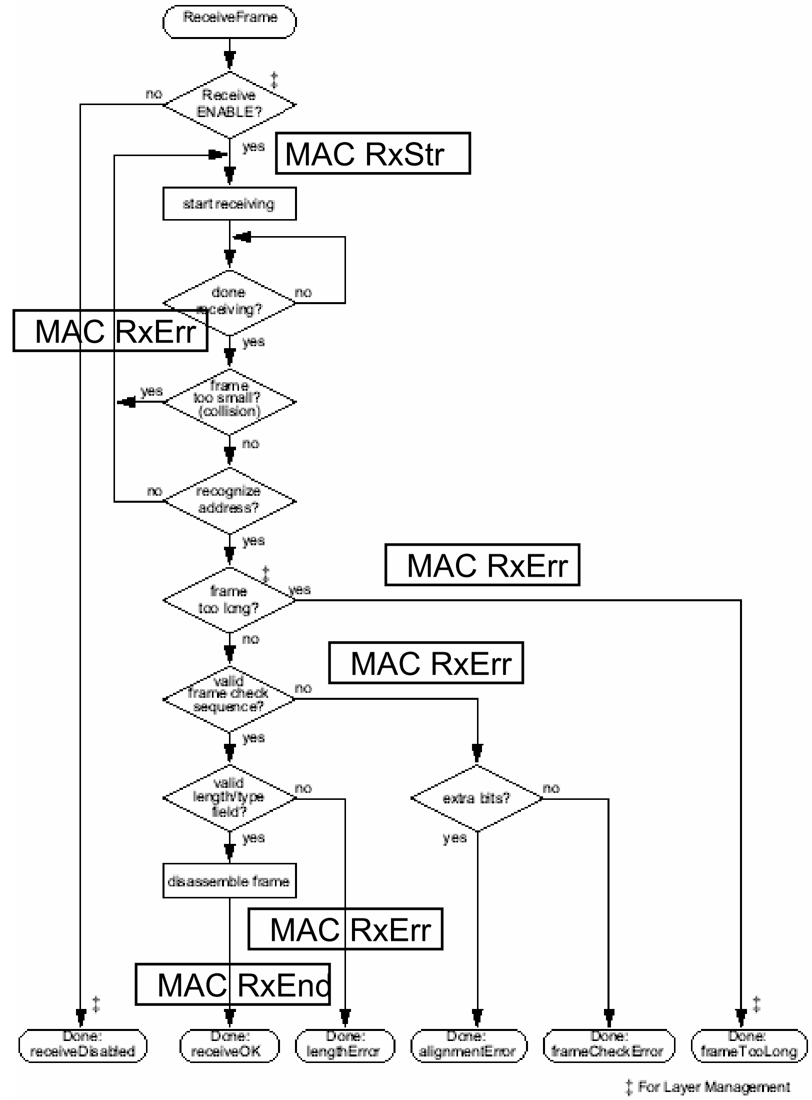
2- MAC layer assumes transmission happens instantly upon PLS_DATA.request(OUTPUT_DATA)

4.2 – Organization of Procedural Model



a) TransmitFrame

Figure 4–2a—Control flow summary

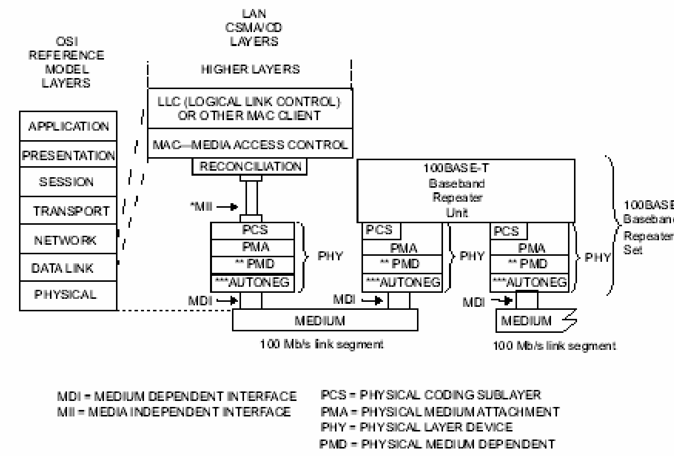


b) ReceiveFrame

Figure 4–2b—Control flow summary

OBS.: Prior to P802.3ar - CM

MAC delays



Clause 21.8

Table 21–2—MAC delay assumptions (exposed MII)

Sublayer measurement points	Event	Min (bits)	Max (bits)	Input timing reference	Output timing reference
MAC ⇔ MII	MAC transmit start to TX_EN sampled		4		TX_CLK rising
	CRS assert to MAC detect	0	8		
	CRS de-assert to MAC detect	0	8		
	CRS assert to TX_EN sampled (worst case nondeferred transmit)		16		TX_CLK rising
	COL assert to MAC detect	0	8		
	COL de-assert to MAC detect	0	8		
	COL assert to TXD = Jam sampled (worst-case collision response)		16		TX_CLK rising; first nibble of jam

Clause 24.6 100BASE-X

Table 24–2—Bit delay constraints

a) MDI to MII delay constraints (exposed MII, half duplex mode)

Sublayer measurement points	Event	Min (bits)	Max (bits)	Input timing reference	Output timing reference
MII ⇔ MDI	TX_EN sampled to MDI output	6	14	TX_CLK rising	1st bit of /J/
	MDI input to CRS assert		20	1st bit of /J/	
	MDI input to CRS de-assert (aligned)	13	24	1st bit of /T/	
	MDI input to CRS de-assert (unaligned)	13	24	1st ONE	
	MDI input to COL assert		20	1st bit of /J/	
	MDI input to COL de-assert (aligned)	13	24	1st bit of /T/	
	MDI input to COL de-assert (unaligned)	13	24	1st ONE	
	TX_EN sampled to CRS assert	0	4	TX_CLK rising	
	TX_EN sampled to CRS de-assert	0	16	TX_CLK rising	

Table 24–3—Bit delay constraints *(continued)*

b) PHY delay constraints (exposed MII, full duplex mode)

Sublayer measurement points	Event	Min (bits)	Max (bits)	Input timing reference	Output timing reference
MII ⇔ MDI	TX_EN sampled to MDI output		14	TX_CLK rising	1st bit of /J/
	MDI Input to RX_DV de-assert		32	first bit of /T/	RX_CLK rising

Table 24–4—DTE delay constraints (unexposed MII, half duplex mode)

Sublayer measurement points	Event	Min (bits)	Max (bits)	Input timing reference	Output timing reference
MAC ⇔ MDI	MAC transmit start to MDI output		18		1st bit of /J/
	MDI input to MDI output (worst-case nondeferred transmit)		54	1st bit of /J/	1st bit of /J/
	MDI input to collision detect		28	1st bit of /J/	
	MDI input to MDI output = Jam (worst case collision response)		54	1st bit of /J/	1st bit of jam

MAC-MDI = 18 bits

MAC delays II

Clause 36.5 1000BASE-X MAC-MDI = 140 bits

Table 36–9a—MDI to GMII delay constraints (half duplex mode)

Sublayer measurement points	Event	Min (bit time)	Max (bit time)	Input timing reference	Output timing reference
GMII ⇔ MDI	TX_EN=1 sampled to MDI output	—	136	PMA_TX_CLK rising	1st bit of /S/
	MDI input to CRS assert	—	192	1st bit of /S/	
	MDI input to CRS de-assert	—	192	1st bit of /K28.5/	
	MDI input to COL assert	—	192	1st bit of /S/	
	MDI input to COL de-assert	—	192	1st bit of /K28.5/	
	TX_EN=1 sampled to CRS assert	—	16	PMA_TX_CLK rising	
	TX_EN=0 sampled to CRS de-assert	—	16	PMA_TX_CLK rising	

Table 36–9b—MDI to GMII delay constraints (full duplex mode)

Sublayer measurement points	Event	Min (bit time)	Max (bit time)	Input timing reference	Output timing reference
GMII ⇔ MDI	TX_EN=1 sampled to MDI output	—	136	PMA_TX_CLK rising	1st bit of /S/
	MDI input to RX_DV de-assert	—	192	1st bit of /T/	RX_CLK rising

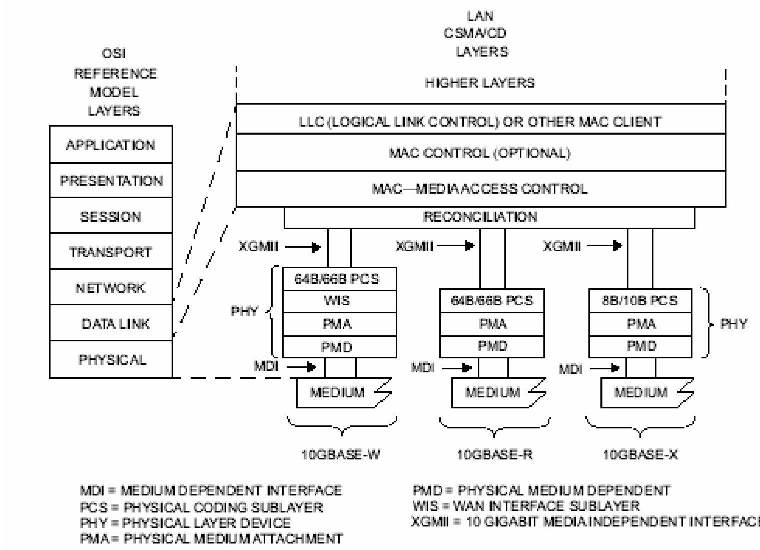


Figure 44–1—Architectural positioning of 10 Gigabit Ethernet

Clause 44.3 XGMII MAC-MDI = ? bits

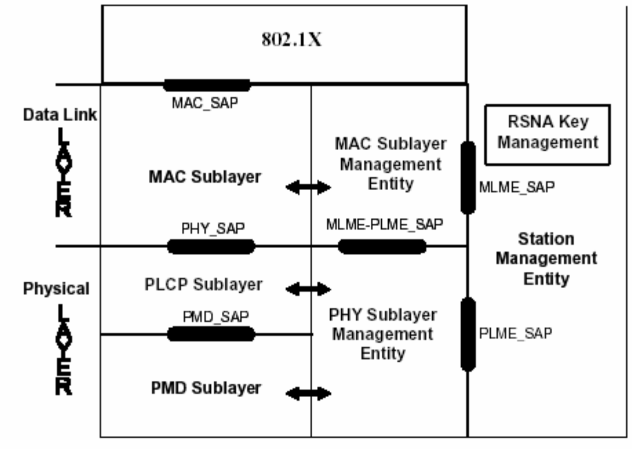
Table 44–2—Round-trip delay constraints (informative)

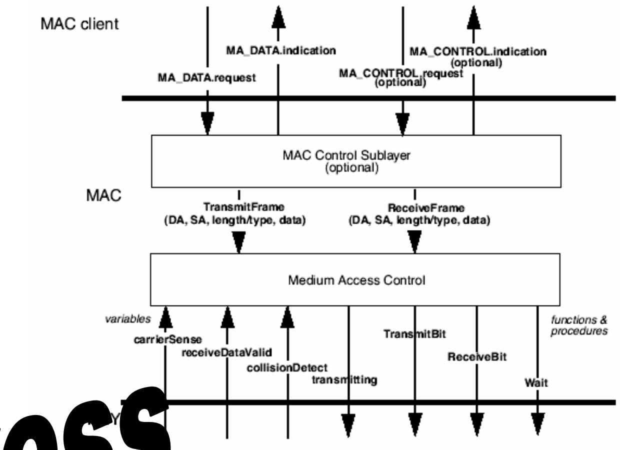
Sublayer	Maximum (bit time)	Maximum (pause_quanta)	Notes
MAC, RS and MAC Control	8192	16	See 46.1.4.
XGXS and XAUI	4096	8	Round-trip of 2 XGXS and trace for both directions. See 47.2.2.
10GBASE-X PCS and PMA	2048	4	See 48.5.
10GBASE-R PCS	3584	7	See 49.2.15.
WIS	14336	28	See 50.3.7.
LX4 PMD	512	1	Includes 2 meters of fiber. See 53.2.
CX4 PMD	512	1	See 54.3.
Serial PMA and PMD	512	1	Includes 2 meters of fiber. See 52.2.

BackUp Slides

BackUp Slides

Time/sync in 802.11 architecture





Work In Progress

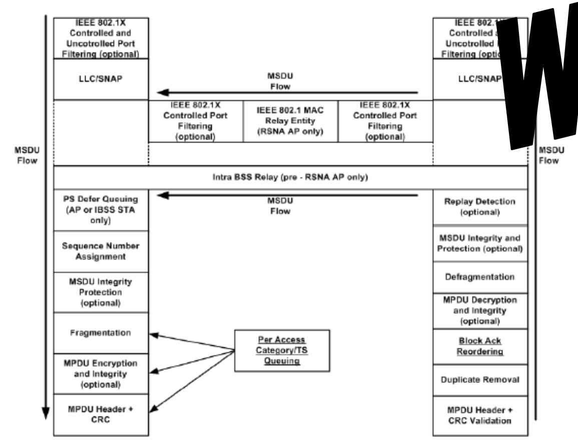


Figure 18—MAC data plane architecture

PLS_DATA.indicate : used for reception timestamp

PLS_DATA.tx : new primitive, for transmission timestamp

Proposal:
-Sync/Followup
-Pdelay/Resp

Proposal:
- Timestamping

dataTx

dataTx

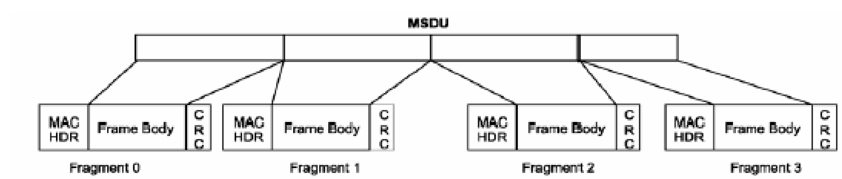


Figure 155—Fragmentation