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Tony Jeffree
IEEE
Chair 802.1 Working Group

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Dear Mr. Jeffree,

In your letter of 16 July, 2009, you asked some questions relating to the reasoning behind some of the jitter requirements that are in SMPTE 259M, SMPTE 292M and SMPTE 424M. The specific answers to your questions follow:

a) Does the maximum frequency drift rate requirement of 0.1 Hz/s apply to the uncompressed digital video signals specified in SMPTE 259M-2008? If it does apply, why does it apply given that it was originally developed to control the frequency drift rate of the analog video color subcarrier?

The requirement does apply. The main reason for the tight frequency specifications is that the SMPTE 259M specification actually describes four different serial interfaces. SMPTE 259 Level A describes an interface in which the analog NTSC signal is sampled with a clock which is at a rate of 14.318 MHz, which is exactly 4x the frequency of the color subcarrier. On the receive end, the expectation is that a clock can be extracted from the serial data stream, and used for a D/A converter which will convert the serial digital data directly back into the original analog signal. Because of this, the timing requirements of the analog video signal were directly transferred to the digital data stream.

b) What is the purpose of the timing jitter requirements in SMPTE 259M-2008, 292M-2008 and 424M-2006 (i.e., what are the requirements attempting to control)? Why are the measurement filter bandwidths as narrow as 10Hz

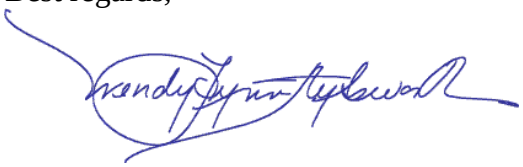
Again, the answer to this relates back to SMPTE 259M Level A, which transfers the timing requirements of the analog signal directly to the SMPTE 259M serial signal. When the newer HD standards (SMPTE 292M) and 3G standards (SMPTE 424M) were developed, SMPTE simply used the existing jitter specifications and measurement methods that had already been documented because they were more than adequate.

In the intervening years since SMPTE 259M was first put into place, several things have changed. Although there are still some SMPTE 259M level A systems in operation, very little, if any, new equipment is being designed to support this standard. Most standard definition SDI equipment today uses SMPTE 259M Level C (270 Mbps) which is less sensitive to clock stability and jitter. Similarly, SMPTE 292M and SMPTE 424M equipment is not as sensitive to clock stability and jitter as is SMPTE 259M level A equipment.

There are two current activities within SMPTE which are looking at this issue. Within the 32NF Technology Committee on Networks and Facilities, there is a Study Group on Jitter Specification and Measurements for Serial Digital Interfaces, which is looking at the existing jitter specifications and determining if they need to be updated in light of the advances in serial digital transmission. Mark Sauerwald is the chair for this study group.

There is also a new Technology Committee TC-33TS on Time Labeling and Synchronization which is chaired by Dr. Hans Hoffmann, which is chartered with the synchronization of systems and essence in both digital and analog forms over both networked and streaming transports. TC-33TS has just recently been formed, so the exact nature of the issues that they will be dealing with has not yet been fully revealed, but they will likely find themselves confronting the same frequency stability requirements that you are asking about.

Best regards,



Cc: Bob Edge – SMPTE 33TS Co-Chair
John Footen – SMPTE 32NF Co-Chair
Geoffrey M. Garner – IEEE
Hans Hoffmann – SMPTE 33TS Chair
Alan Lambshead – SMPTE 32NF Chair
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