Ethernet Timestamping
Precision/Accuracy

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Analog Devices
Clocks/Relationships

- Grand Master Rate Ratio
- Working Clock
- Local Clock
- Neighbor Rate Ratio
- PTP Stack (slave)
- Sync Messages
- Peer Delay Measurement
- Comms Clock
- PTP Stack (master)
- Grand Master Rate Ratio
- Working Clock
- Local Clock
- Neighbor Rate Ratio
- PTP Stack (slave)
- Comms Clock
- Sync Messages
- Peer Delay Measurement
Timestamp Points/Signals

RGMII/GMII-1000Base-T Timestamping

Egress Timestamp

Rx Clock Transition (Jitter)

Rx PHY Delay

Tx Clock Transition (Jitter)

Tx PHY Delay

Cable Delay

Tx PHY Delay

Rx Clock Transition (Jitter)

Ingress Timestamp
Synchronization Points

- PHY Communication Clocking
- Chrystal Oscillator
- Switch Clocking
- RGMII/GMII Receive Path
- Sync FIFO
- Receive MAC
- Rx Timestamp
- Tx Timestamp
- MII Transmit Path
- Sync FIFO

Syntonized Clock

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Summary

► Typical implementation minimizes magnitude and number of clock frequencies
► Typical MAC/port clock frequency in the neighborhood of 125 Mhz (Gbit support)
► MII is the only standard interface that provides high frequency information of transmit timing
  ▪ MII doesn’t support Gbit operation and is unpopular due to high pin count
► To support timestamp precision greater than 8 nsec:
  ▪ Need additional signaling from the PHY to bridge on transmit path
    ▪ Non-standard. Existing implementations differ (and most don’t support preemption).
  ▪ Need higher frequency logic or custom capture unit to sample timing signals (both tx and rx)
  ▪ Need to integrate information from high precision signal logic into timestamp generation units