IEEE/IEC 60802 cTE introduction

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Introduction

- The presentation (Further Analysis of cTE Budgeting for an IEC/IEEE 60802 Network, Based on Multiple Replication dTE simulations with Variable Intermessage Intervals) provided some consideration about time error budget allocation, including dTE (dynamic Time Error) and cTE (constant Time Error)
- The definition of cTE and dTE are specified in ITU-T G.8260
 - cTE: the constant component of the time error sequence, could be averaged with the time error sequence
 - dTE: the dynamic component (random noise) of the time error sequence, could be expressed by the peak-to-peak, MTIE or TDEV of the time error sequence.

Introduction

• This slide gives a simpler explanation on how to get cTE and dTE.



Step 2: Estimate dTE (e.g., peak-to-peak) and cTE (averaging).

Factors of cTE

- The cTE could be caused by fiber asymmetry, or PTP devices.
- Internal delay 2 • For PTP devices, the factors include the asymmetry of timestamp generation, internal delay compensation or others. MAC MAC MAC Timestamp generation point PHY PHY RX TΧ RX TΧ PHY delay – 1 PHY Link Link RX TX Link **SLAVE MASTER** port port

Local clock

1 : PHY needs to report its RX and TX delay to the MAC layer, and the delays or the asymmetry should be compensated to generate the timestamps at the MAC layer

2 : The delay from the local clock to the timestamping clock at MAC layer should be measured and compensated.

However, even after compensation, some error could still be present, and a fully ideal compensation is not practical.

Several possible implementations



CTE should be smaller for case 1, case 2, and case 3 respectively.

Summary

- The cTE specification of PTP relay and PTP end station should be carefully considered.
- A cTE value less than 5ns could be achievable for case 1, i.e.; Slave and Master ports are from one chip.

Thank you