$ETHERNOVI\Delta$

TRANSFORMING HOW CARS OF THE FUTURE ARE BUILT

IEEE802.1DG – TDMA MODES

2021-05-11

ADDITIONAL AFFILIATIONS: BMW, RUETZ SYSTEM SOLUTIONS



IEEE contribution



35 NOTE 1—Since the origin of the PTP timescale is 1 January 1970 00:00:00 TAI, CycleStartTime will be larger than 36 1.3×10^{18} ns. If sufficient precision is not maintained when computing N, CycleStartTime will not be an integer 37 multiple of OperCycleTime, which could result in misalignment of the cycles at ports on different bridges.

Open Open Open Open Open	Open Closed Closed Closed Closed
Closed Closed Closed Closed	Closed Open Closed Closed Closed
Open Open Open Open Open	Closed Closed Open Closed Closed
Closed Closed Closed Closed	Closed Closed Closed Open Closed
Open Open Open Open Open	Closed Closed Closed Open

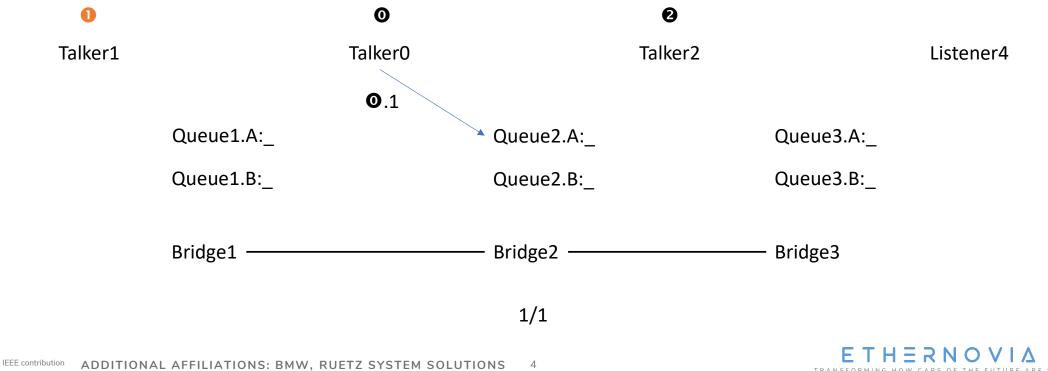
Looking at the one Gate a specified Frame will encounter through the network.

H = S N O V I V

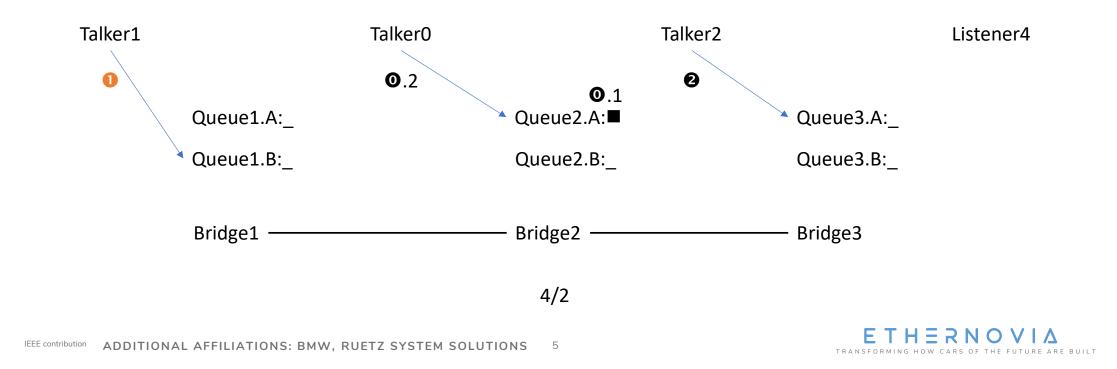
A very simple network model

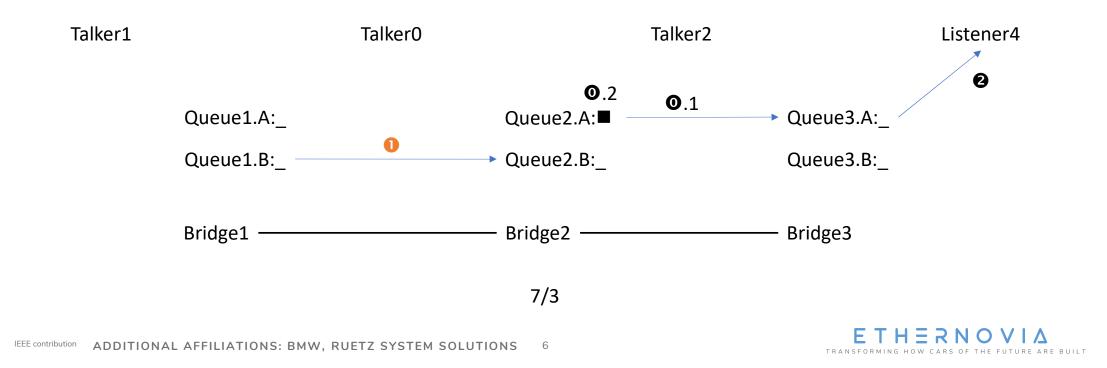
Starting without any TDMA

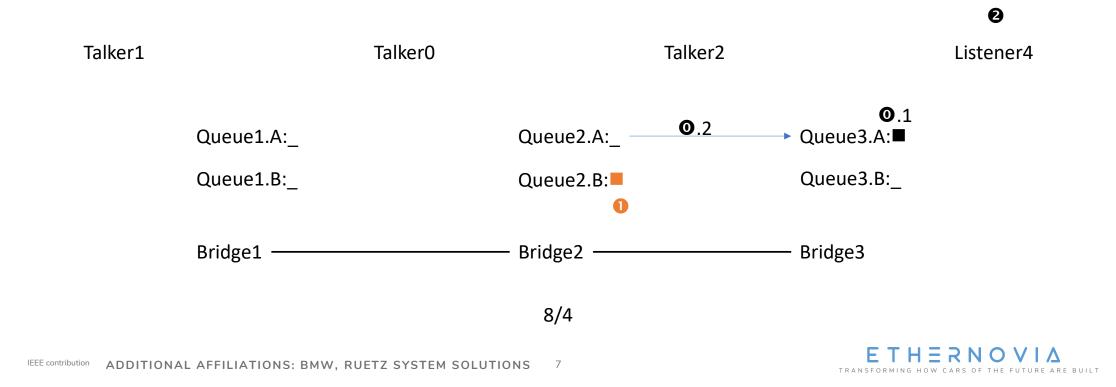
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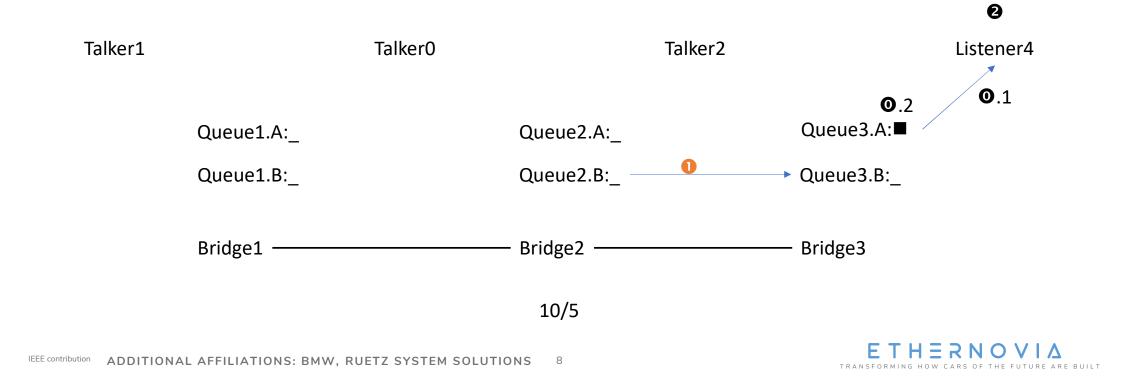


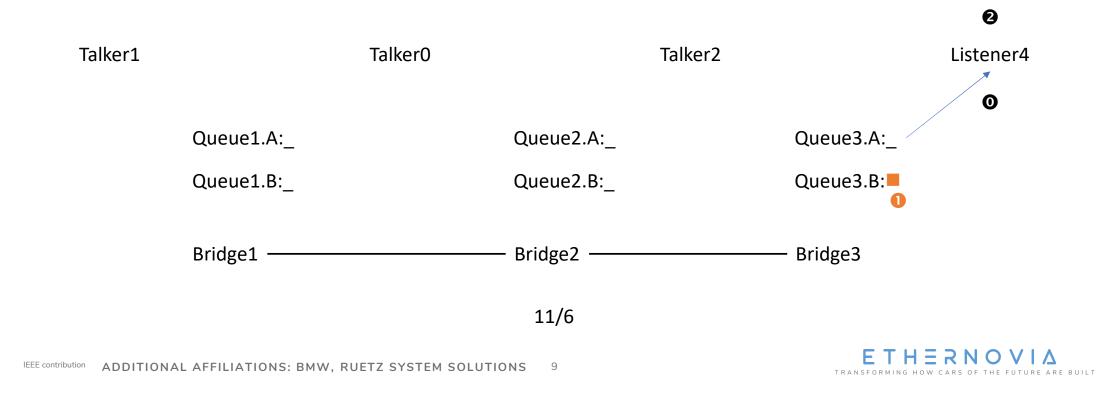
4 SEORMING HOW CARS OF THE EUTURE ARE BUILT

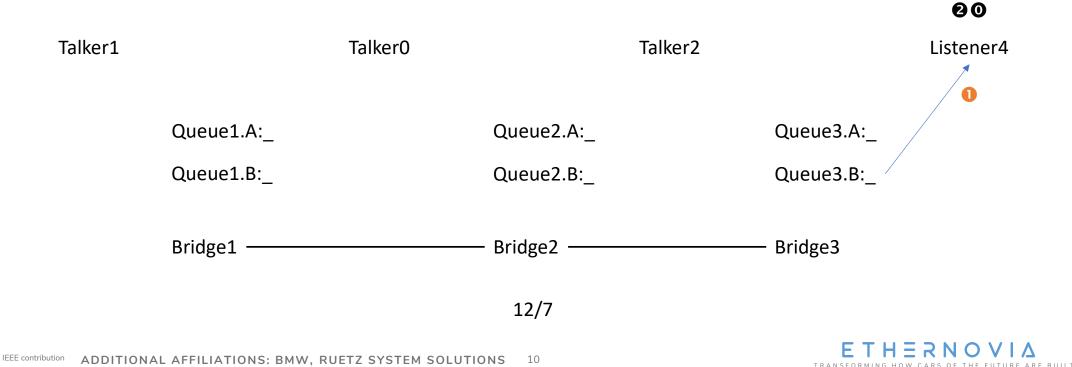












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Bus-Mode TDMA

The FlexRay timing model on switched Ethernet

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IEEE802.1Q-2018 8.6.9.1.1 SetCycleStartTime()

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Bus-Mode TDMA

Open Open Open Open Open

Closed Closed Closed Closed

Open Open Open Open Open

Closed Closed Closed Closed

Open Open Open Open Open

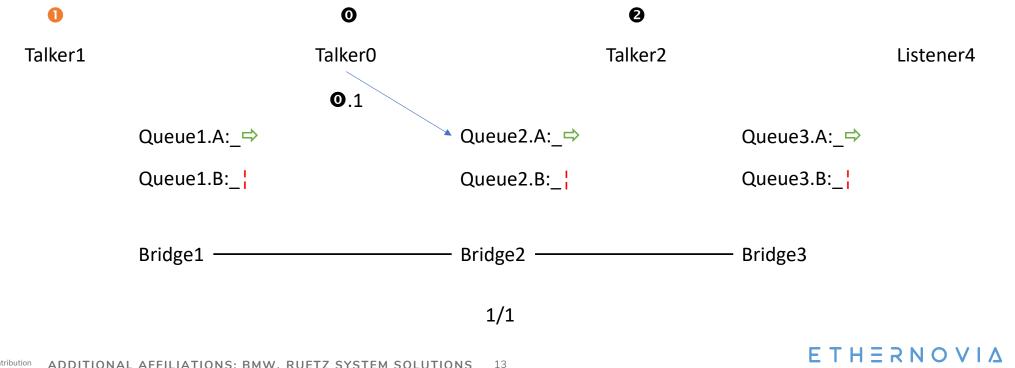
Open Closed Closed Closed Closed Closed Open Closed Closed Closed Closed Closed Open Closed Closed Closed Closed Closed Open Closed

Closed Closed Closed Open

Looking at the one Gate a specified Frame will encounter through the network.

time

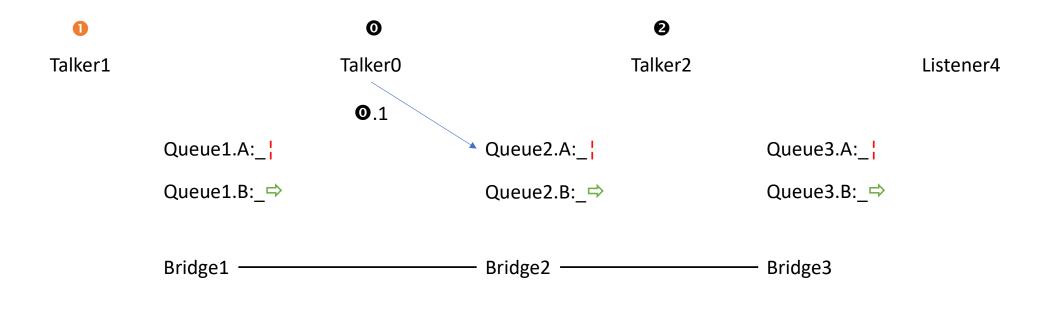




IEEE contribution ADDITIONAL AFFILIATIONS: BMW, RUETZ SYSTEM SOLUTIONS

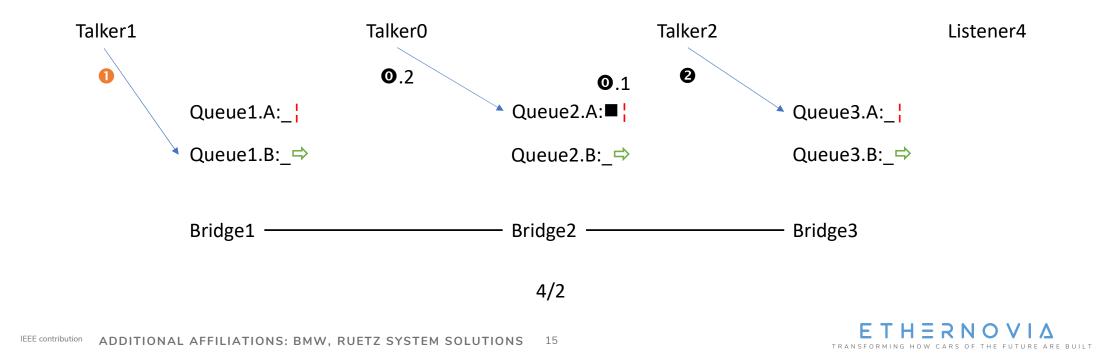
SEORMING HOW CARS OF THE EUTURE ARE BUILT

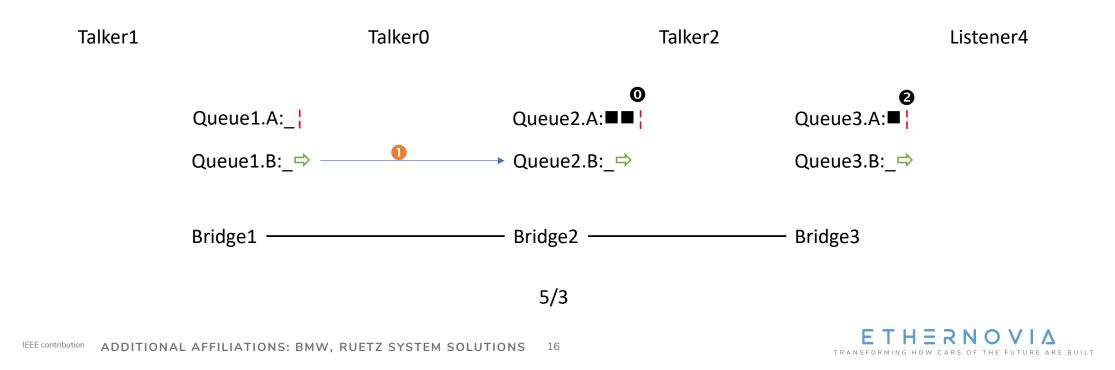
System-Wide Guard-Band Queue#.A Start!

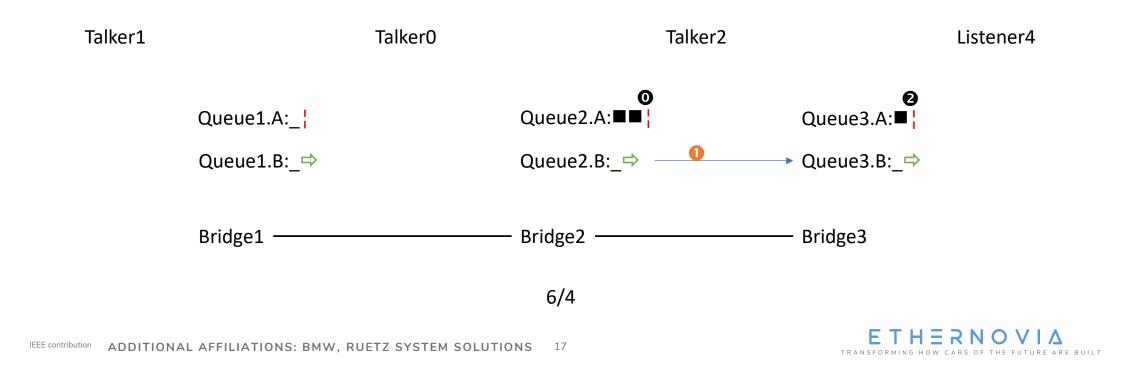


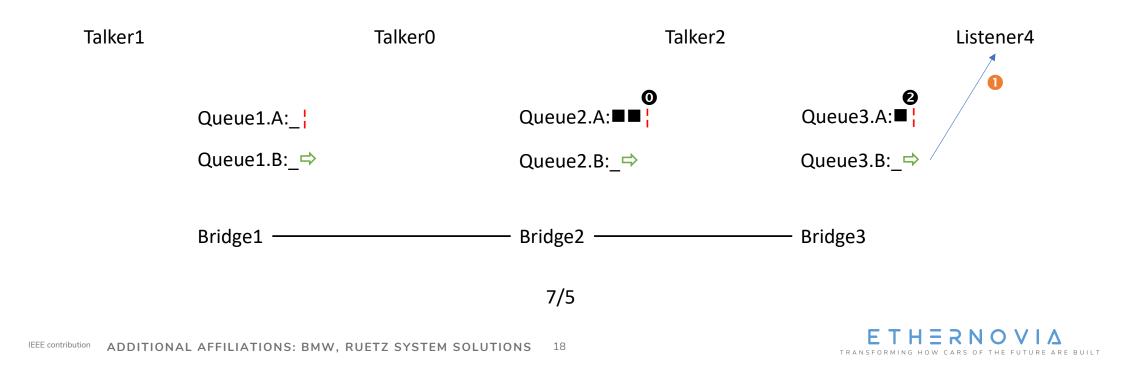
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SEORMING HOW CARS OF THE EUTURE ARE BUILT

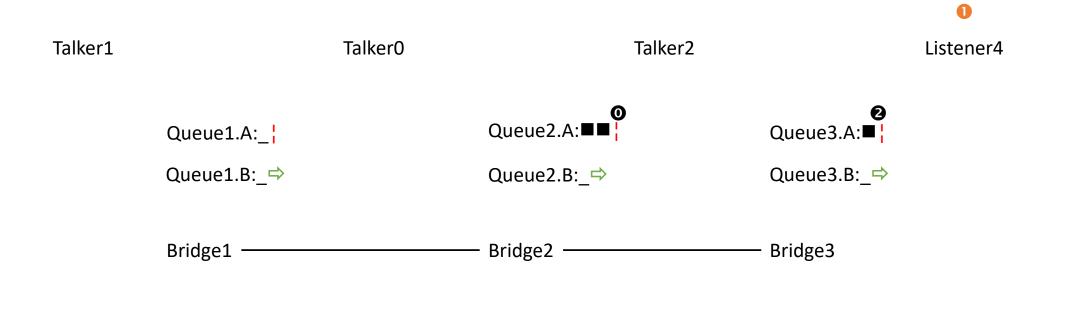






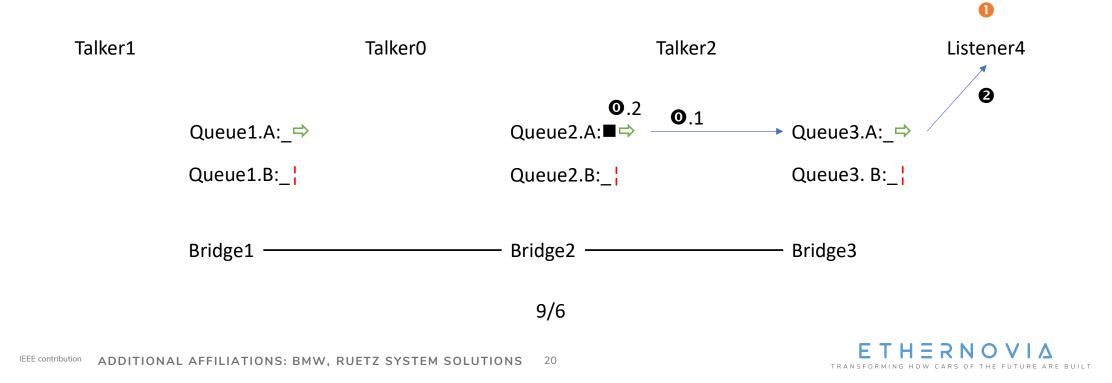


Tolerance Band





All Queue#.A open back up.



Phased-Mode TDMA

"La Ola the wave" on switched Ethernet



IEEE802.1Q-2018 8.6.9.1.1 SetCycleStartTime()

35 NOTE 1—Since the origin of the PTP timescale is 1 January 1970 00:00:00 TAI, CycleStartTime will be larger than 36 1.3×10^{18} ns. If sufficient precision is not maintained when computing N, CycleStartTime will not be an integer 37 multiple of OperCycleTime, which could result in misalignment of the cycles at ports on different bridges.

Open	Open	Open	Open	Open

Closed Closed Closed Closed

Open Open Open Open Oper

Closed Closed Closed Closed

Open Open Open Open Open

Phased-Mode TDMA

Open Closed Closed Closed Closed

Closed Open Closed Closed Closed

Closed Closed Open Closed Closed

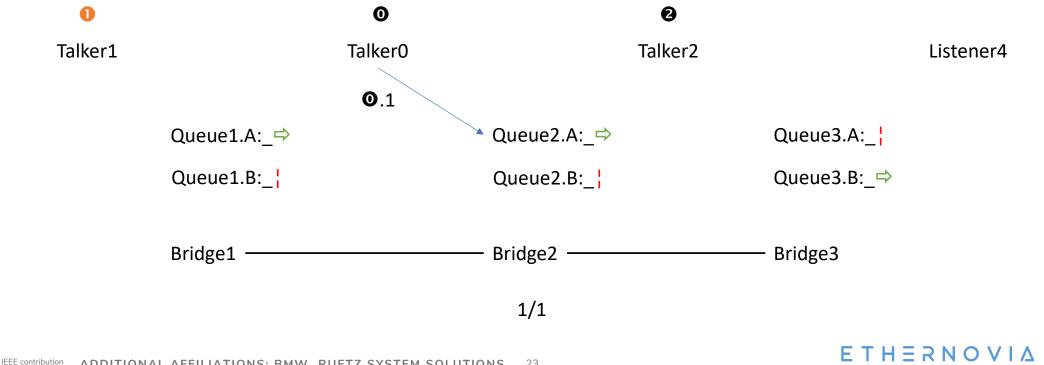
Closed Closed Closed Open Closed

Closed Closed Closed Open

F Τ Η = R Ν Ο V Ι Δ

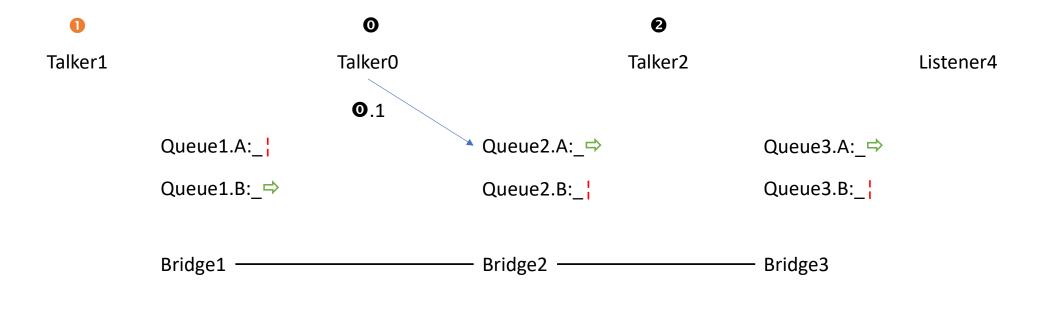
Looking at the one Gate a specified Frame will encounter through the network.

time



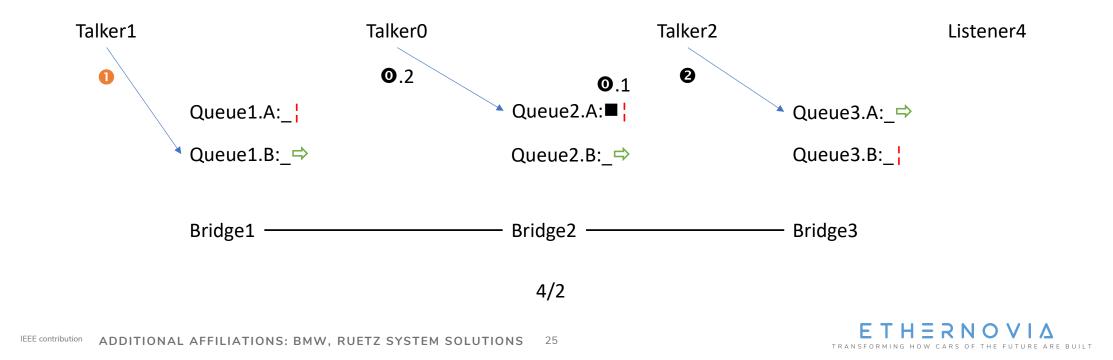
ADDITIONAL AFFILIATIONS: BMW, RUETZ SYSTEM SOLUTIONS 23 RMING HOW CARS OF THE EUTURE ARE BUILT

Guard-Band Start on Queue1.A!

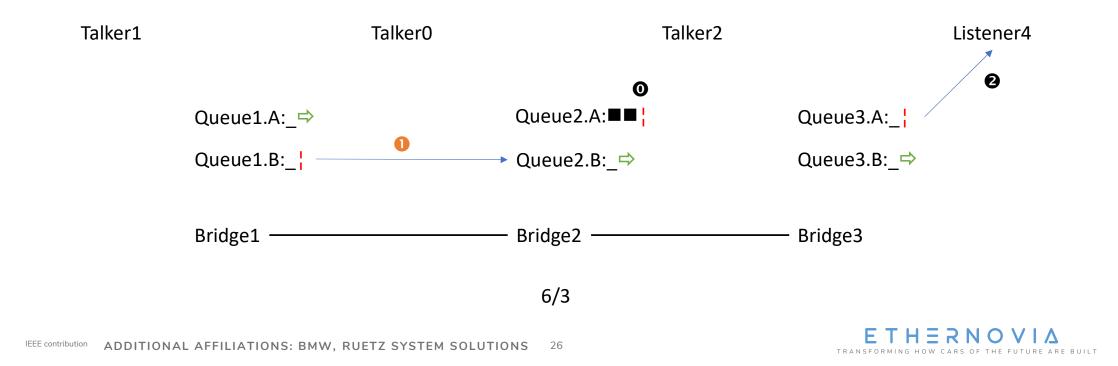


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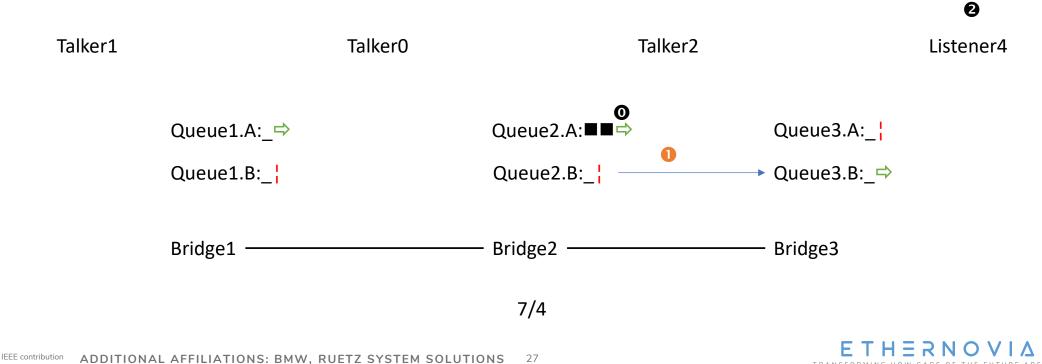
Guard-Band Start on Queue2.A!



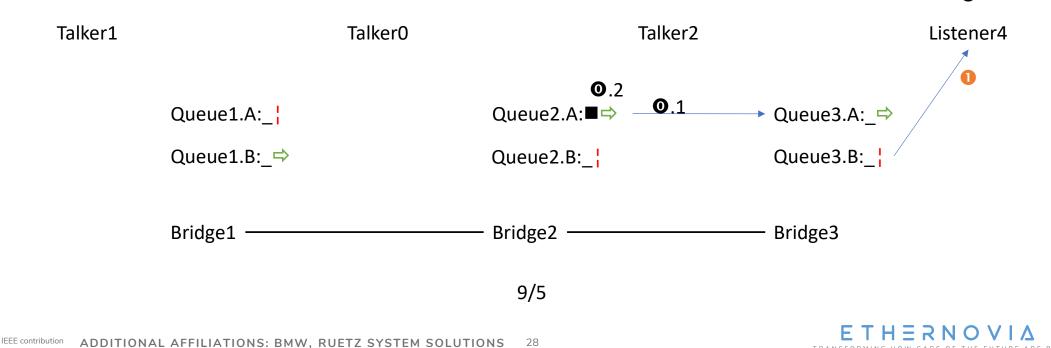
Guard-Band Start on Queue3.A! Queue1.A can open up after Tolerance-Band!



Queue2.A can open up after Tolerance-Band!



Queue3.A can open up after Tolerance-Band!



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Conclusions

As the models are very simple, these conclusions are more of an indication than a hard result



Conclusions

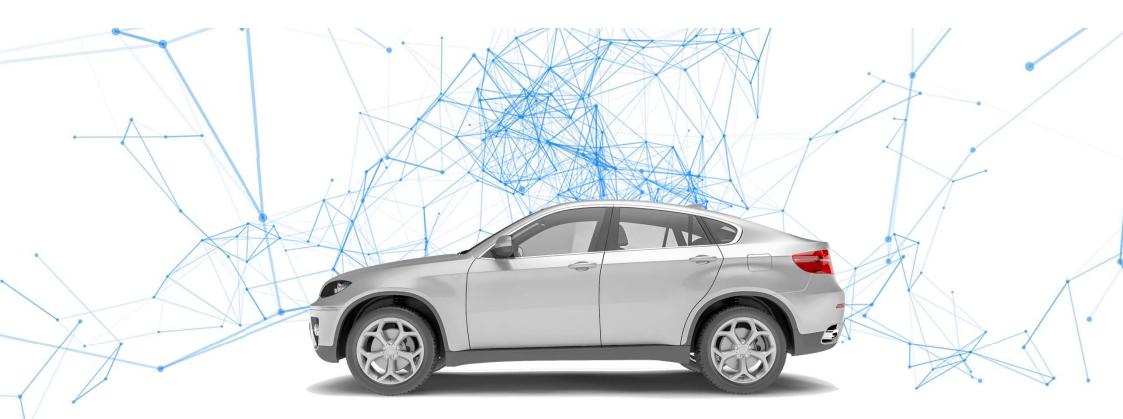
• The Bus-Mode TDMA

- does provide a delivery on time guarantee
- is rather inefficient on a system wide scale
- makes Gate-Timing system-wide parameter
- will suffer from timing inaccuarcy

• The Phased-Mode TDMA

- does provide a delivery on time guarantee
- is more efficient on a system wide scale than Bus-Mode
- makes Gate-Timing a per-hop parameter
- requires even better timing accuracy than Bus-Mode





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ADDITIONAL AFFILIATIONS: BMW, RUETZ SYSTEM SOLUTIONS



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