MAC and PHY delay variation

Impact of MAC and PHY jitter

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MAC and PHY model

Time stamping for synchronization faces a difference between the model and the reality.

While the model assumes he timestamping point at the MDI, the real timestamping is mainly done „before“ the MAC.
PHY model

Values from manufacturer:

MII to MDI latency
- Transmit direction
- Receive direction

Latency variation (See 802.3cx)
- Min and Max
  - Transmit
  - Receive
802.3 – PHY located between xMII and MDI
P802.3cx
– Transmit and Recieve latency variation

Table 45–140—TimeSync PMA/PMD transmit path data delay register

<table>
<thead>
<tr>
<th>Bit(s)</th>
<th>Name</th>
<th>Description</th>
<th>R/Wa</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.1801.15:0</td>
<td>Maximum PMA/PMD transmit path data delay in ms, lower</td>
<td>PMA/PMD_delay_ms_TX_max [15:0]</td>
<td>RO, MW</td>
</tr>
<tr>
<td>1.1802.15:0</td>
<td>Maximum PMA/PMD transmit path data delay in ms, upper</td>
<td>PMA/PMD_delay_ms_TX_max [31:16]</td>
<td>RO, MW</td>
</tr>
<tr>
<td>1.1803.15:0</td>
<td>Minimum PMA/PMD transmit path data delay in ms, lower</td>
<td>PMA/PMD_delay_ms_TX_min [15:0]</td>
<td>RO, MW</td>
</tr>
<tr>
<td>1.1804.15:0</td>
<td>Minimum PMA/PMD transmit path data delay in ms, upper</td>
<td>PMA/PMD_delay_ms_TX_min [31:16]</td>
<td>RO, MW</td>
</tr>
<tr>
<td>1.1809.15:0</td>
<td>Maximum PMA/PMD transmit path data delay in sub-ns</td>
<td>PMA/PMD_delay_subns_TX_max [15:0]</td>
<td>RO</td>
</tr>
<tr>
<td>1.1810.15:0</td>
<td>Minimum PMA/PMD transmit path data delay in sub-ns</td>
<td>PMA/PMD_delay_subns_TX_min [15:0]</td>
<td>RO</td>
</tr>
</tbody>
</table>

Table 45–141—TimeSync PMA/PMD receive path data delay register

<table>
<thead>
<tr>
<th>Bit(s)</th>
<th>Name</th>
<th>Description</th>
<th>R/Wa</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.1805.15:0</td>
<td>Maximum PMA/PMD receive path data delay in ms, lower</td>
<td>PMA/PMD_delay_ms_RX_max [15:0]</td>
<td>RO, MW</td>
</tr>
<tr>
<td>1.1806.15:0</td>
<td>Maximum PMA/PMD receive path data delay in ms, upper</td>
<td>PMA/PMD_delay_ms_RX_max [31:16]</td>
<td>RO, MW</td>
</tr>
<tr>
<td>1.1807.15:0</td>
<td>Minimum PMA/PMD receive path data delay in ms, lower</td>
<td>PMA/PMD_delay_ms_RX_min [15:0]</td>
<td>RO, MW</td>
</tr>
<tr>
<td>1.1808.15:0</td>
<td>Minimum PMA/PMD receive path data delay in ms, upper</td>
<td>PMA/PMD_delay_ms_RX_min [31:16]</td>
<td>RO, MW</td>
</tr>
<tr>
<td>1.1811.15:0</td>
<td>Maximum PMA/PMD receive path data delay in sub-ns</td>
<td>PMA/PMD_delay_subns_RX_max [15:0]</td>
<td>RO</td>
</tr>
<tr>
<td>1.1812.15:0</td>
<td>Minimum PMA/PMD receive path data delay in sub-ns</td>
<td>PMA/PMD_delay_subns_RX_min [15:0]</td>
<td>RO</td>
</tr>
</tbody>
</table>

aRO = Read only, MW = Multi-word.
PHY model: Parameter example

Example (best in class):

- 100Mbit/s
- TX latency (const) = 100ns
- TX latency (var) = 0...4ns
- RX latency (const) = 180ns
- RX latency (var) = 0...4ns

Example (random):

- 100Mbit/s
- TX latency (const) = 100ns
- TX latency (var) = 0...32ns
- RX latency (const) = 180ns
- RX latency (var) = 0...16ns
MAC model: Parameter example

**Example (best in class):**

100Mbit/s
TX latency (const) = some value
TX latency (var) = 0
RX latency (const) = some value
RX latency (var) = 0

That’s the remaining delay of
- the MAC after the real time stamp point and xMII for transmit
- the MAC after the xMII and the real time stamp point for receive
Problem statement: Synchronization

Example 1:
Timestamping error = timestamp itself (4ns/8ns) + uncertainty MAC latency (0ns) + uncertainty PHY latency (4ns) = 12ns

Example 2:
Timestamping error = timestamp itself (4ns/8ns) + uncertainty MAC latency (32ns) + uncertainty PHY latency (125ns) = 165ns

Timestamp error influences the - Pdelay value - Residence time value

Additionally, the asymmetry of errors is a problem
Questions 1/2

What are the values for the MAC delay variations?

For the selected
- 10Mbit/s MAU Types
- 100Mbit/s MAU Types
- 1Gbit/s MAU Types
- 2,5Gbit/s MAU Types
- 5Gbit/s MAU Types
- 10Gbit/s MAU Types
Questions 2/2

What are the values for the PHY delay variations?
For the selected
- 10Mbit/s MAU Types
- 100Mbit/s MAU Types
- 1Gbit/s MAU Types
- 2,5Gbit/s MAU Types
- 5Gbit/s MAU Types
- 10Gbit/s MAU Types
Summary

MAC and PHY delay variation influences

- Pdelay measurement erroneous
  - Delay value is the average value if filtering is applied
- Pdelay measured vs. real sync message pdelay
  - Different frames do have different pdelay (inside the min/max of MAC/PHY delay)
- Residence time measurement erroneous
  - Delay variation creates uncertainty when the frame is (and was) at the reference point (compared to the real timestamping point)

Used algorithms need to take these errors into account!
Questions?