Feedback Control in Time/Clock Synchronization

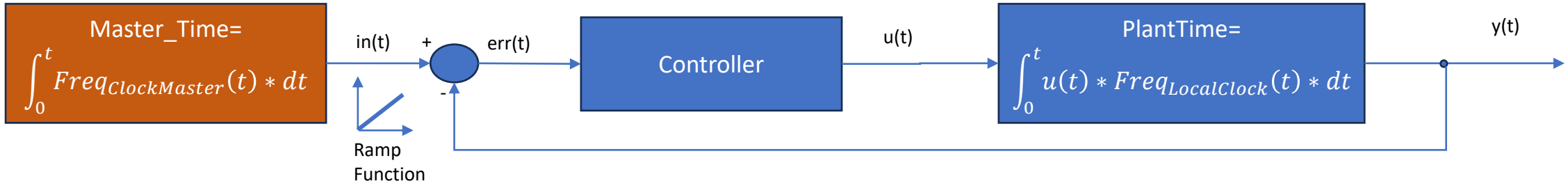
Dragan Obradovic

Siemens AG

Continuous Time/Clock Control Loop

- The control loop gets the best local estimate of the Master Time delivered by Sync Messages (with compensated propagation delay) and tries to follow it
- Since Sync messages arrive periodically, the control loop is effectively discrete time
- The control signal (output of the controller) scales the integral of the frequency of the local free running clock, i.e. Local-Clock, producing the Control Time y(t)

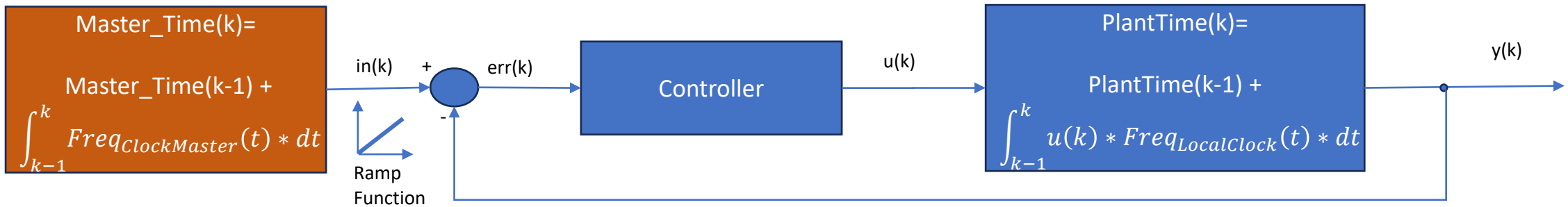
- **We can also describe a fictitious continuous time version of this control loop:**



- The input signal in(t) is the Master Time, i.e. the integral of the ClockMaster frequency. It is a ramp signal whose derivative is the mentioned frequency
- The output signal y(t) is the Controlled Master Time (the best tracking of in(t)). It is also a ramp signal.
- The plant is the integral of the frequency of the Local-Clock, hence it generates a time (a counter value) signal. In the open-loop case (with u(t)=1), the output signal y(t) is actually the time/clock_counter value of the Local-Clock.

Time-Discrete version of the Time/Clock Control Loop

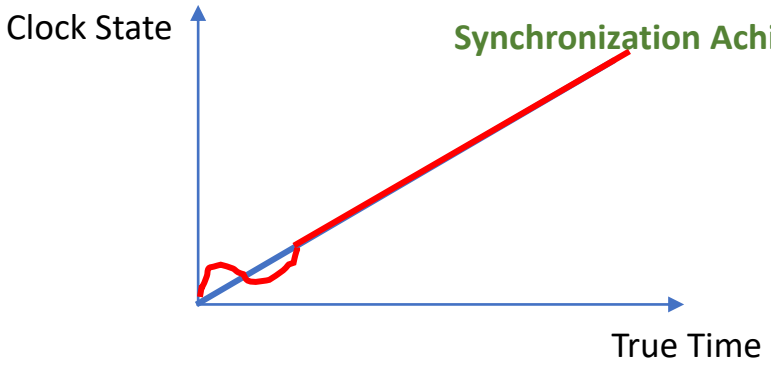
- The time sampling is triggered by the Sync message arrivals, with Tsync sampling rate
- Let “k-1” and “k” be the times of the arrival of the Sync messages with these indices



- The input signal in(k) is the Master Time, i.e. the integral of the ClockMaster frequency. It is in the time-discrete case a step-wise function.
- The output signal y(k) is the Controlled Master Time (the best tracking of in(k)). It is also a time discrete ramp signal (step-wise increasing signal)
- The plant is the integral of the frequency of the Local-Clock.

Achieved Synchronization

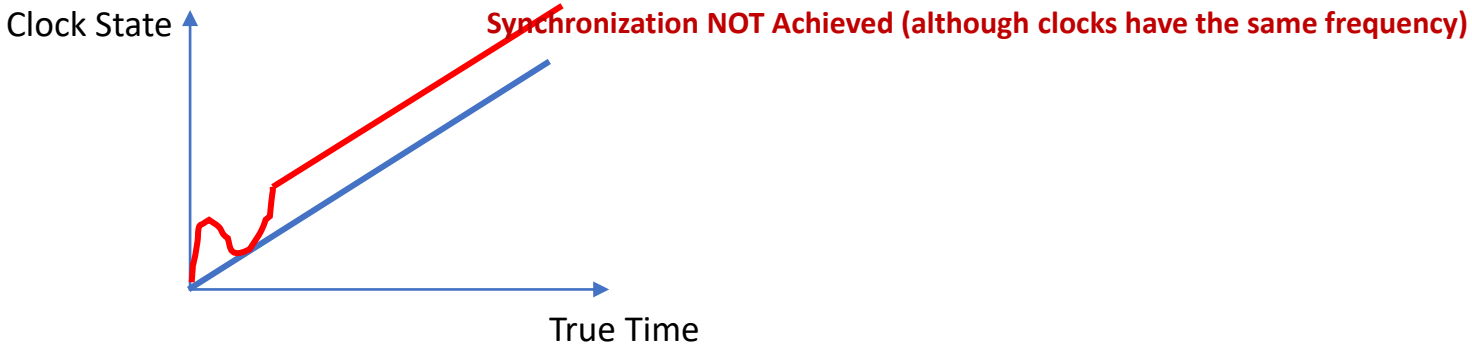
CASE 1: **Synchronization is achieved**, we will have the following dependency of the followed Master time (clock counter value) and the control loop time (clock counter value):



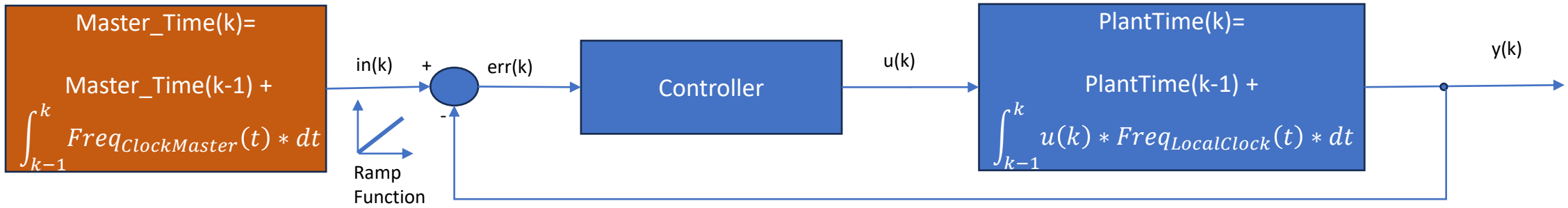
- Blue: the reference signal (Master-Clock Time)
- Red: the control signal (the Control Time)

- **➔ after some transient time, two signals (ramps) are identical!**
- **➔ the underlying oscillators have the same frequency and zero phase difference**

CASE 2: **Synchronization NOT achieved although the control time has the same frequency & phase as the reference Master Time.** ➔ Equalizing the rates (frequencies) of these two clocks is NOT enough (this is what a PLL would normally do). <u>But clocks need to have identical counter values!</u>

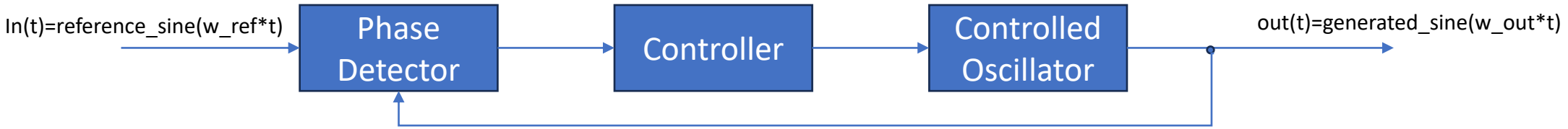


Properties of the Time/Clock Control Loop



- The input and the output signals to the control loop are ramp signals (time or clock values) and not sine or cosine signals.
- These signals are obtained by integrating frequencies of the corresponding frequencies.
- In the time discrete case, we observe the passed time/clock_counter values in the sampling interval (defined by arrival of Sync messages). Hence no explicit estimation of the frequency is necessary.
- The control signal (depending on implementation) remains constant within the sample interval.
- If we would like to talk about some phase difference, here this would be the difference between two time ramp signals.
- But this control loop will not be a classic PLL whose input and outputs should be periodic signals.

Typical PLL (to my knowledge)



- The input and the output signals to PLL are periodic signals like sine functions.
- The phase detector is usually not a simple sum or difference of the input signals. It can actually be based on the product of the reference and the output signal, which is a non-linear operation.

- in time/Clock synchronization we do not change the frequency of an oscillator directly (as above) but only its integral in a given time interval by adding or subtracting a certain number of tics (time units).