[May, 2026]

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Relation between IEEE P802.1AS and IEEE Std 82.3 PHY delay

IEEE 802 Interim Meeting, May 2026, Munich, Germany

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contribution to

IEEE

Denoting Interfaces incl. IEEE Std 802.3 Clause 90

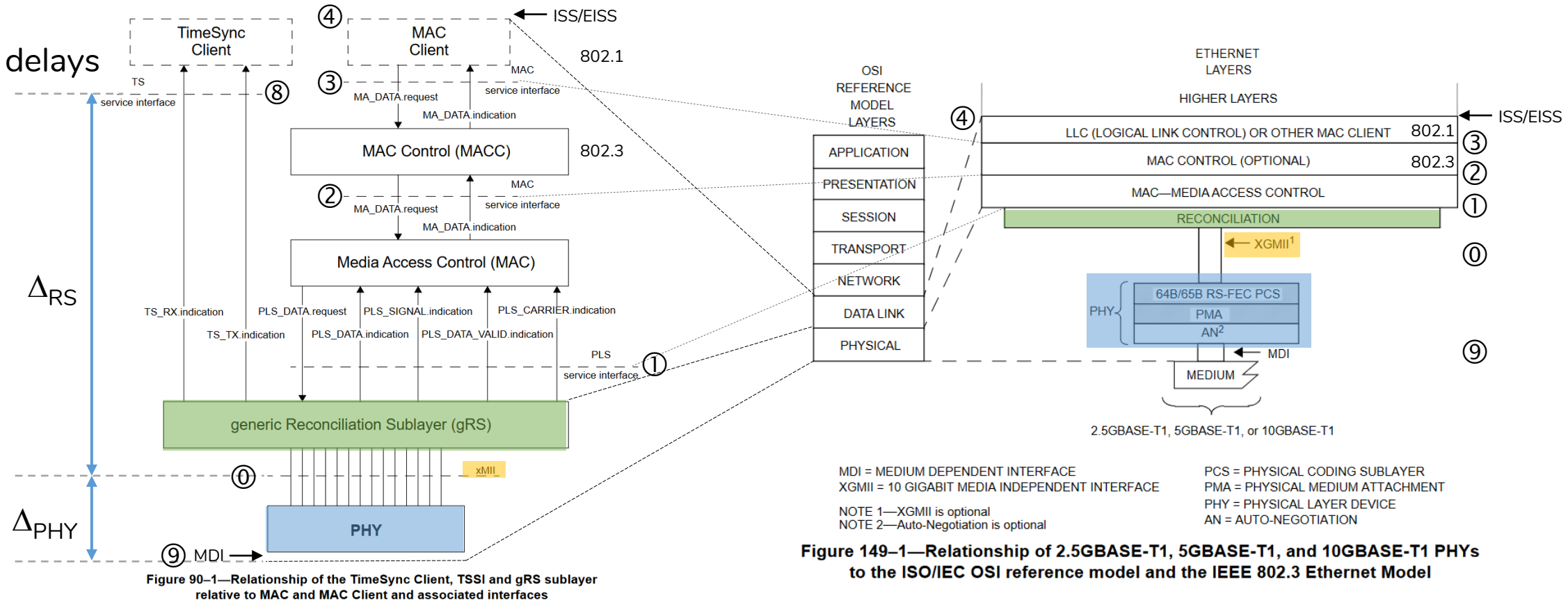

Figure 90–1—Relationship of the TimeSync Client, TSSI and gRS sublayer relative to MAC and MAC Client and associated interfaces

Figure 149–1—Relationship of 2.5GBASE-T1, 5GBASE-T1, and 10GBASE-T1 PHYs to the ISO/IEC OSI reference model and the IEEE 802.3 Ethernet Model

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gRS – xMII – PHY

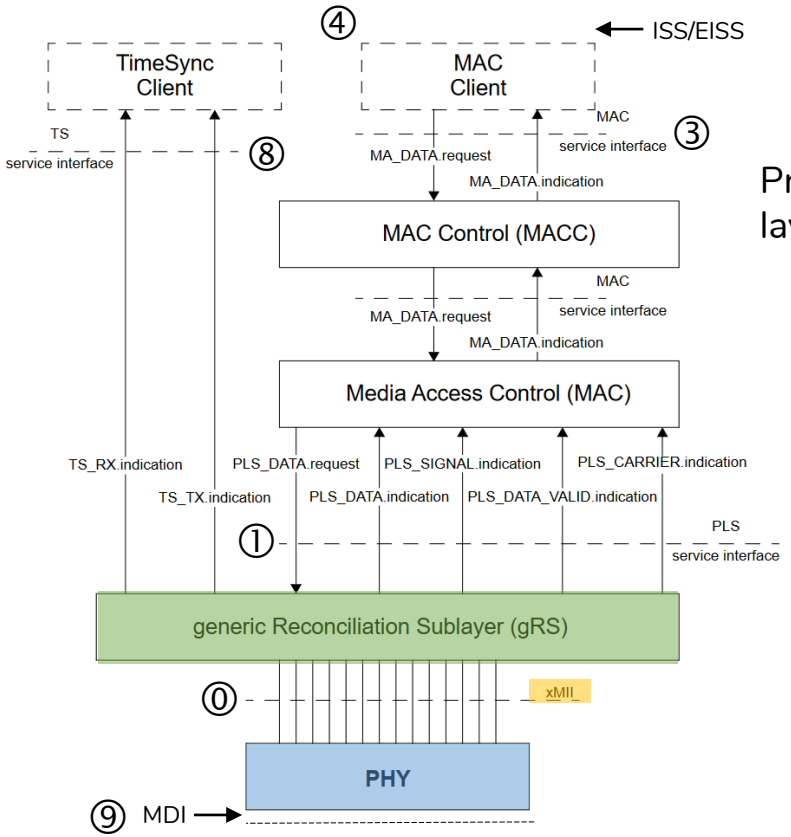
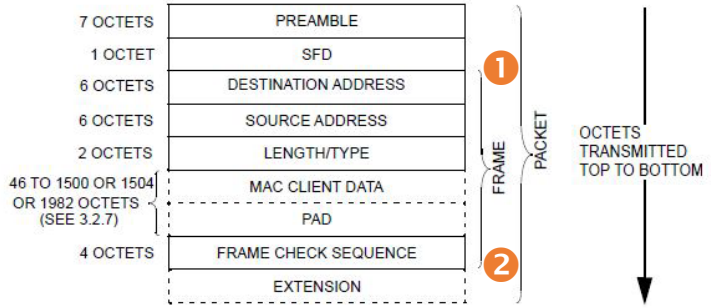
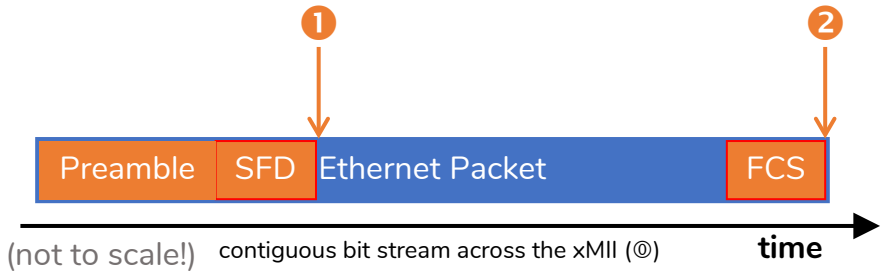


Figure 90–1—Relationship of the TimeSync Client, TSSI and gRS sublayer relative to MAC and MAC Client and associated interfaces

Processing through the MAC model layers is not considered here!



Below the (g)RS (at ⓪) the time between ❶ and ❷ (T_{MII}) is given by <the number of bits contained in the Ethernet Frame> (L) divided by <the nominal bit rate[1)] of the xMII> (R_{MII})



The bit stream across the xMII (at ⓪) is contiguous for TX and RX, independent of Interleaving

[1)] 802.3:1.4.213 bit rate (BR)

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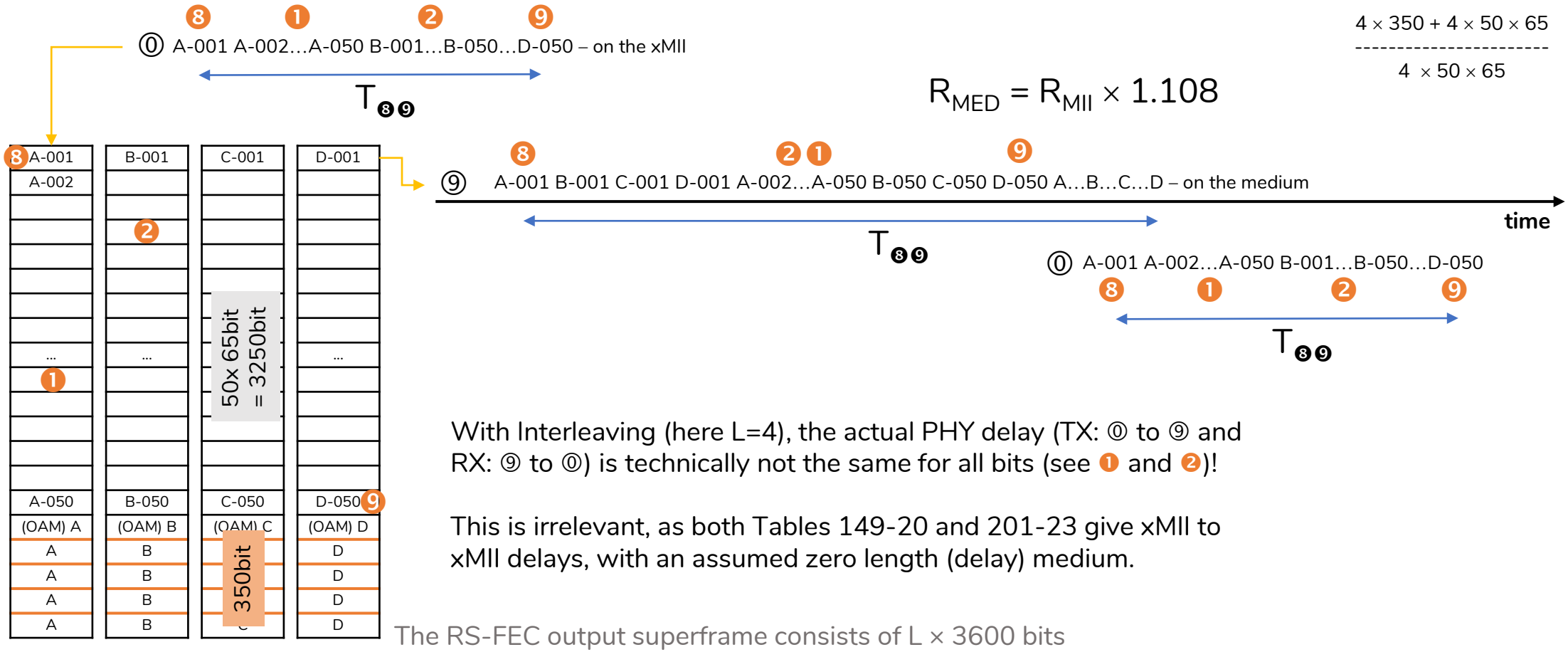
IEEE Std 802.3CH - Interleaving

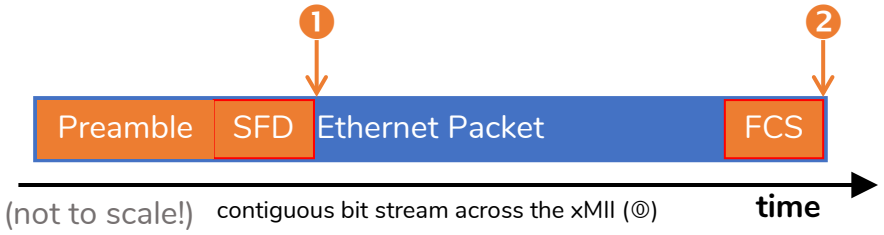


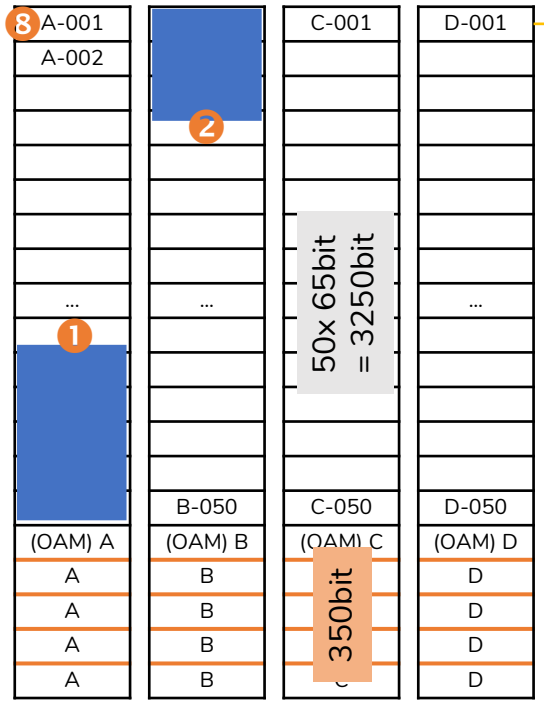
With Interleaving (here L=4), the actual PHY delay (TX: ⓪ to ⑨ and RX: ⑨ to ⓪) is technically not the same for all bits (see ❶ and ❷)!

This is irrelevant, as both Tables 149-20 and 201-23 give xMII to xMII delays, with an assumed zero length (delay) medium.

The RS-FEC output superframe consists of L × 3600 bits

IEEE Std 802.1AS and PHY Interleaving





8 2 1 9

A-001 B-001 C-001 D-001 A-002…A-050 B-050 C-050 D-050 A…B…C…D – on the medium

This does not make “physical” sense for Interleaving!

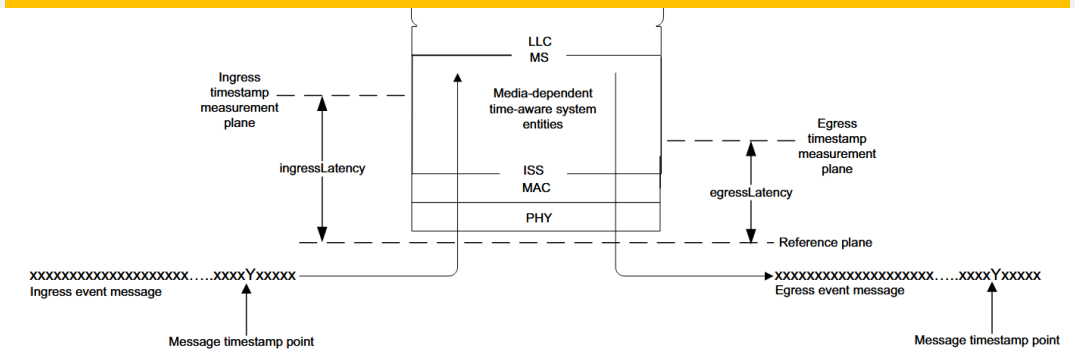


Figure 8-2—Definition of message timestamp point, reference plane, timestamp measurement plane, and latency constants

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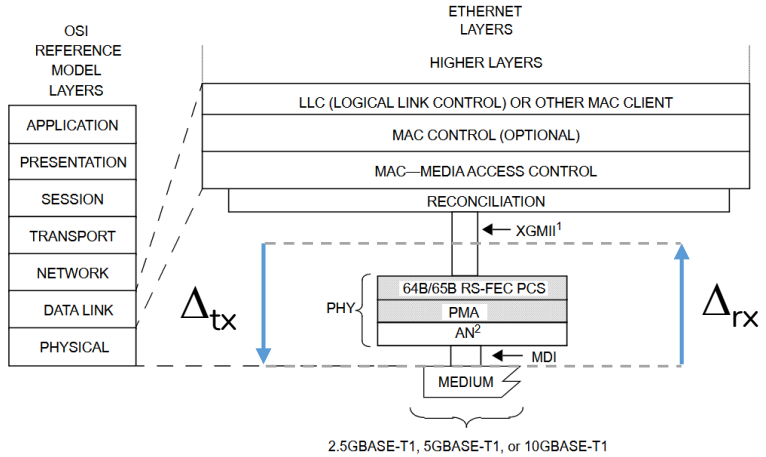
IEEE Std 802.3CH – Section 149.10 Delay Limits

149.10 Delay constraints

In full duplex mode, predictable operation of the MAC Control PAUSE operation (Clause 31, Annex 31B) also demands that there be an upper bound on the propagation delays through the network. This implies that MAC, MAC Control sublayer, and PHY implementers conform to certain delay maxima, and that network planners and administrators conform to constraints regarding the cable topology and concatenation of devices.

The sum of the transmit and receive data delays for an implementation of the PHY shall not exceed the limits shown in Table 149–20. Transmit data delay is measured from the input of a given unit of data at the XGMII to the presentation of the same unit of data by the PHY to the MDI. Receive data delay is measured from the input of a given unit of data at the MDI to the presentation of the same unit of data by the PHY to the XGMII.

NOTE—The physical medium interconnecting two PHYs introduces additional delay in a link.



per line-item:

$\Delta_{CH}[M,I] > \Delta_{tx} + \Delta_{rx}$

Table 149–20—Delay Limits

Mode	Interleave	Bit times	Pause Quanta	Delay (ns)
2.5GBASE-T1	1x	10 240	20	4096
5GBASE-T1	1x	10 240	20	2048
5GBASE-T1	2x	13 824	27	2764.8
10GBASE-T1	1x	10 240	20	1024
10GBASE-T1	2x	13 824	27	1382.4
10GBASE-T1	4x	20 480	40	2048

MAC Control PAUSE Operation IEEE Std 802.3CH

$d_{Total} = d_{Pause} + (d_{TA} + d_W + d_{RB}) + d_{React} + d_{MTU} + (d_{TB} + d_W + d_{RA})$

$d_{Total} = (d_{TA} + d_{RA}) + (d_{TB} + d_{RB}) + (d_{Pause} + d_{React} + d_{MTU} + 2d_W)$

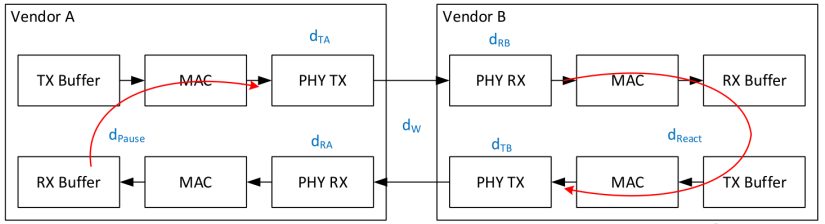
- Regroup transmit and receive of each path to be from same device

$d_{Total} = d_A + d_B + d_O$

Where:

- d_A and d_B are PHY Delay limit specified by IEEE (i.e. Clause 149.10) reported by vendor

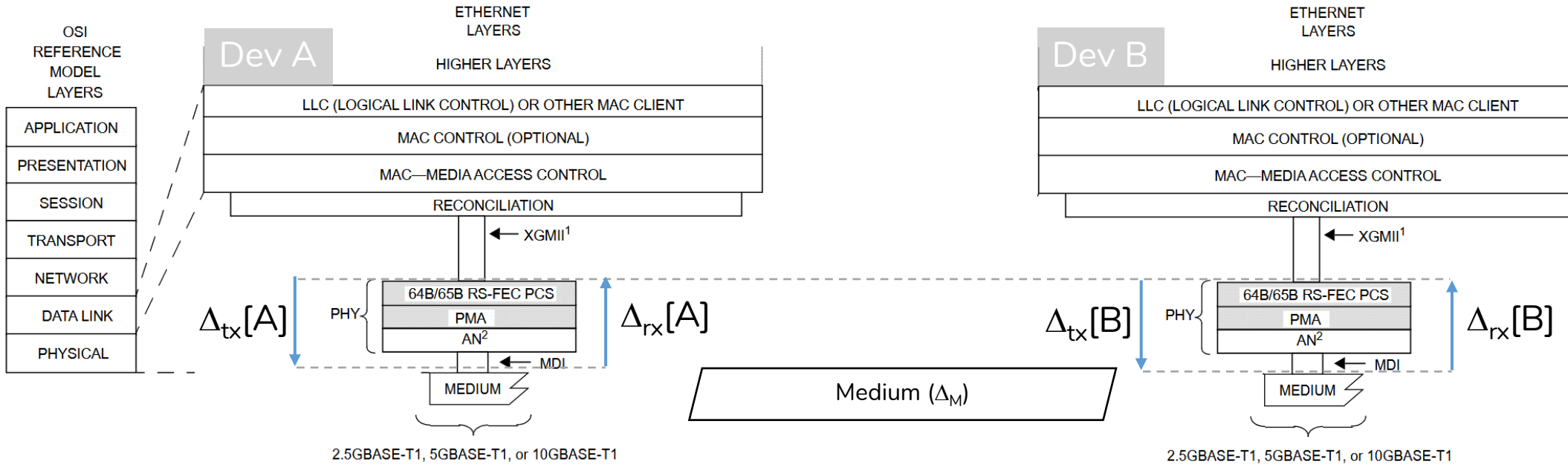
- d_{Pause} RX buffer high water mark to pause frame generated on XGMII
- d_{React} Pause frame received on XGMII to TX buffer stopping traffic
- d_{TA}, d_{TB} XGMII to MDI PHY delay for vendor A and B
- d_{RA}, d_{RB} MDI to XGMII PHY delay for vendor A and B
- d_W Wire propagation delay. Assumed to be the same both direction
- d_{MTU} Duration of maximum size packet



https://www.ieee802.org/3/dm/public/0326/Lo_3dm_01_030926.pdf

Because the PAUSE control information passes through each PHY once in TX and once in RX direction, only the sum (as specified in .3CH) of the two is relevant!

Clause 90 TimeSync with IEEE Std 802.3CH - MultiGig



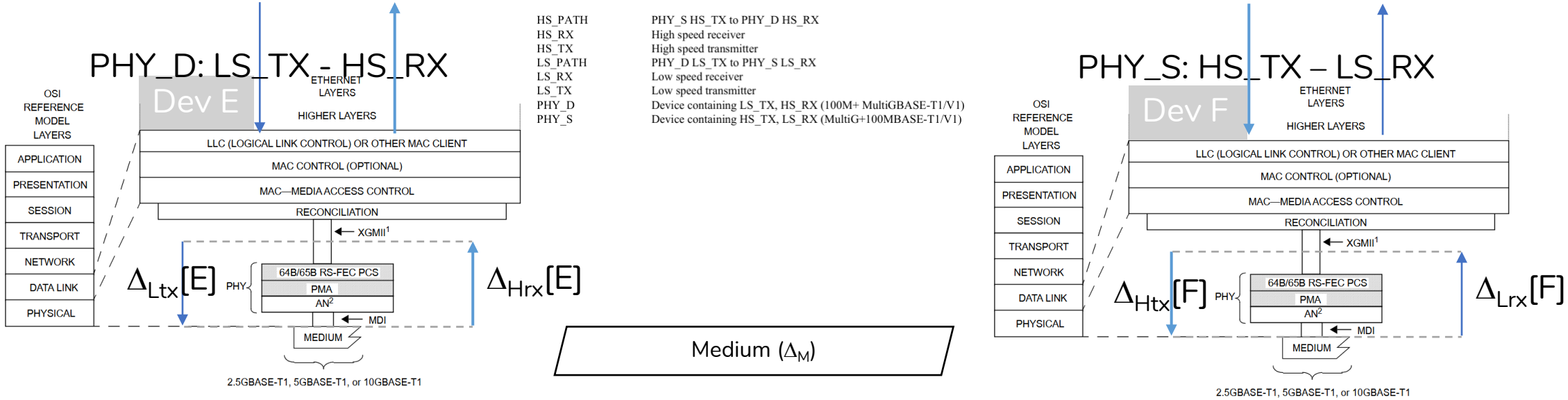
pDelay requested by A:

$$\Delta_{pDelay} = \Delta_{RS}[A] + \Delta_{tx}[A] + \Delta_M + \Delta_{rx}[B] + \Delta_{RS}[B] + \Delta_{react}[B] + \Delta_{RS}[B] + \Delta_{tx}[B] + \Delta_M + \Delta_{rx}[A] + \Delta_{RS}[A]$$

Latency of a Sync-Message from A to B:

$$\Delta_{Sync} = \Delta_{RS}[A] + \Delta_{tx}[A] + \Delta_M + \Delta_{rx}[B] + \Delta_{RS}[B]$$

Clause 90 TimeSync with IEEE P802.3dm – Asymmetric Ethernet



pDelay requested by E:

$$\Delta_{pDelay} = \Delta_{RS}[E] + \Delta_{Ltx}[E] + \Delta_{M} + \Delta_{Lrx}[F] + \Delta_{RS}[F] + \Delta_{react}[F] + \Delta_{RS}[F] + \Delta_{Htx}[F] + \Delta_{M} + \Delta_{Hrx}[E] + \Delta_{RS}[E]$$

Latency of a Sync-Message from E to F:

$$\Delta_{Sync} = \Delta_{RS}[E] + \Delta_{Ltx}[E] + \Delta_{M} + \Delta_{Lrx}[F] + \Delta_{RS}[F]$$

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IEEE Std 802.1AS

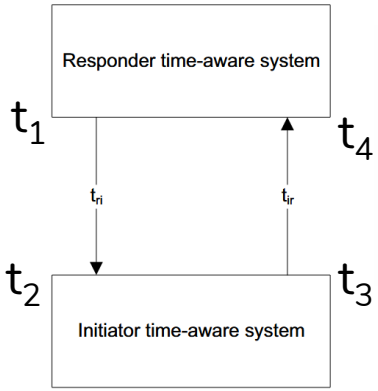

Figure 8-1—Propagation asymmetry

egressTimestamp = egressMeasuredTimestamp + egressLatency

ingressTimestamp = ingressMeasuredTimestamp – ingressLatency

where the timestamps relative to the reference plane, egressTimestamp and ingressTimestamp, are computed from the timestamps relative to the timestamp measurement plane, egressMeasuredTimestamp and ingressMeasuredTimestamp, respectively, using their respective latencies, egressLatency and ingressLatency. Failure to make these corrections results in a time offset between the timeReceiver and timeTransmitter clocks.

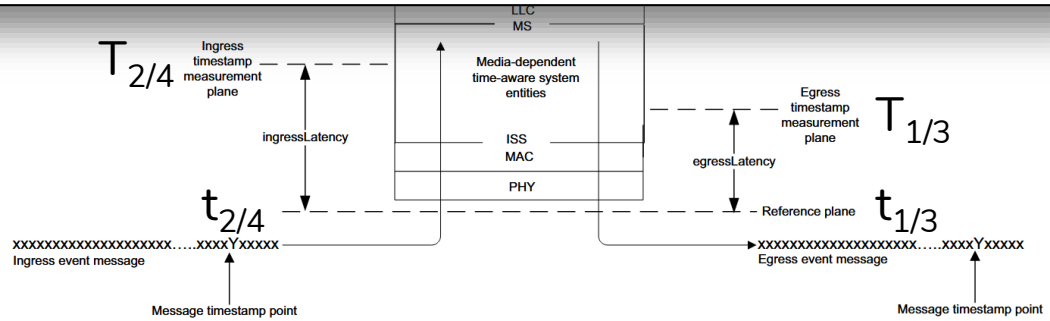

Figure 8-2—Definition of message timestamp point, reference plane, timestamp measurement plane, and latency constants

The meanLinkDelay is the mean value of t_{ir} and t_{ri}, i.e., meanLinkDelay = (t_{ir} + t_{ri}) / 2. The delayAsymmetry is defined as:

t_{ir} = meanLinkDelay – delayAsymmetry

t_{ri} = meanLinkDelay + delayAsymmetry

$$dA = (t_{ri} - t_{ir})/2$$

$$t_{ir} = t_2 - t_1$$
$$t_{ri} = t_4 - t_3$$
$$D = \frac{t_{ir} + t_{ri}}{2} = \frac{(t_4 - t_1) - (t_3 - t_2)}{2} \quad (11\text{-}1)$$

This does not make “physical” sense for Interleaving!

$$D = mLD = ((T_2 - iL[x]) - (T_1 + eL[y]) + (T_4 - iL[y]) - (T_3 + eL[x]))/2$$

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Conclusion

- For PHYs with RS-FEC and Interleaving, the PHY delay (µs) by far exceeds the propagation delay on the wire (5ns/m) for automotive use-cases
- The delayAsymmetry defined in IEEE Std 802.3AS:8.3 only accounts for the on wire propagation, as all timestamps are mapped to the MDI according to 8.4.3
- While for MAC Control PAUSE Operation in IEEE Std 802.3, the sum of TX and RX delays is sufficient for symmetric MultiGig (.3CH), it is insufficient for asymmetric Ethernet (.3dm)
- For IEEE 802.1AS we always need(ed) the one-way delay to correct Sync message timestamps. This can not be measured at the MDI for PHYs with RS-FEC and Interleaving
- One proposal could be to move the reference plane of IEEE Std 802.1AS to the .3 Clause 90 service interface and thereby include the PHY in the meanLinkDealy as well as in the asymmetry considerations
- Otherwise we should coordinate with 802.3 to have definitions and measuremnets for the values required in .1AS

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