# IEEE 802.11 Wireless Access Method and Physical Layer Specifications

TITLE: A Draft Proposal for Direct Sequence Spread Spectrum PHY Standard

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Introduction: This paper proposes a Direct Sequence Spread Spectrum (DSSS) physical layer that operates at 2.4 GHz ISM band. To support a single MAC/multiple PHY interface, the proposed specification have parameters similiar to those proposed in the Frequency Hopping systems.

The specification is put in a table format as long as it is a living document.

### **Requirements outline:**

- Compliance with 802.11 PAR.
- Compliance with Regulatory Agencies for unlicensed operation.
- Support operation in a multinetwork environment. (multiple collocated networks)
- Minimum area coverage.
- Suitable for low power consumption implementations.
- Suitable for small size implementation
- Cost effective
- Ensure interoperability between conformant DSSS stations.
- Modes of operation:
  - peer to peer
  - node to AP and AP to node
- Support asychnronous and time deterministic services.
- Robust operation in narrow band and partial band interference as well as multipath fading
- Graceful degradation under load and interference

## **Specifications:**

The following table uses a template made by Nathan Silberman in the IEEE P802.11-92/127r for the 2.4GHz ISM band. The following table represents a template for DSSS PHY specification. Several areas are left to be determined after the channel model is agreed and after MAC-PHY interface is determined. Other parameters have to be worked out between PHY and MAC groups.

	Parameter	Proposed	Notes	
1.	Frequency range	2.4 - 2.4835 GHZ (USA) 2.4 - 2.5 GHZ (ETSI) 2.471 - 2.497 GHZ (Japan)		
2.	Max. transmitted power level	250 mw	IEEE c.95.1-1991	
3.	Min. transmitted power level	1 mw		
4.	Power control	above 100 mw		
5.	Level of power controls	4 levels	2-bit control	
6.	Number of Channels	3	1 channel for Japanese market	
7.	Data rate	1 M bit /sec	support fallback data rates. see also #8, #10.	
8.	Spreading chip ratio	>= 12, programmable	maintain same channel bandwidth with different data rate. i.e. #7 * #8 is constant.	
9.	Modulation	Binary MSK	modulation index 0.5	
10.	*Receiver Demodulator	Two methods: a. FM descriminator b. Coherent receiver	<ul><li>a. For Post-despreading.</li><li>b. For classical despreading.</li></ul>	
11.	Spreading sequence (main code )	16 bits, 64k length	Choose from sets of Maximal linear code. Longer code makes the information less susceptible to undesirable interception.	
12.	** Spread code preamble: synchornisztion code ( sync code )	5 bits, 31 chips, repeat with inverted sync code for total of 120 us duration.	For code synchronization, antenna selection.	
13.	Channel bandwidth	18 MHZ		
14.	Maximum Radiated EIRP	Controlled by regulatory agencies.		
15.	Spurious emissons in band	TBD		

16.	Spurious emissions out of band	Controlled by regulatory agencies.	
17.	Transmitted power variation	TBD	
18.	Frequency tolerance	100 ppm	
19.	Minimum receiver sensitivity	-80 dBm	at #23 BER.
20.	Adjacent channel rejection margin	40 dB	
21.	Switching time Tx to Rx	20 usec max	
22.	Switching time Rx to Tx	20 usec max	
23.	BER (Bit error rate)	1*10e-7	
24.	Minimum reception distance	50 ft.	
25.	Maximum reception distance	1000 ft.	
26.	Channel availability	99.5%	
27.	Antenna impedence	50 Ω	
28.	Interface lines to convergence layer (when exposed)	a. RX data b. TX data c. RX/TX clock d. RTS/CTS e. Data valid f. Control line g. Status line h. Ctl/Sta Clock	

29. PHY-MAC management info/control variables  a. PHY type (FH, DS or IR)  b. Number of frequency channels c. Signal quality d. Number of RX signal strength levels e. Current RX signal strength f. Number of TX power level h. Set TX power level i. Channel in use (if more than one) j. Sleep mode k. Wake-up l. Standby mode m. Data rate n. Jabber control function o. Jabber indication  30. VSWR  Device shall stand infinite transmit VSWR without damage.  31. Receiver noise figure  32. Safety Requirements  Compliance with applicable Safety Agencies requirements  33. DTE/DCE interface  TBD  TBD				
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			requirements	
34. ACK protocol support TBD	33.	DTE/DCE interface	TBD	
	34.	ACK protocol support	TBD	

#### **Notes:**

## \* Receiver demoulator:

The direct sequence system can have two different versions of receiver design, target for different market requirements. One is post-despreading, which is economical approach at minimum cost and least real-estate on the circuit board. The other one is the classical despreading, which has better jamming margin and processing gain. Certainly, the latter is costly to build. These two versions should be inter-operable.

# \* \*Code structure and Data frame Alignment:

←	120 us	$\rightarrow$		
31 chips	• • •	31chips		
Sync code	• • •	Sync code	Main Code	