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Wireless Access Methods and Physical Layer Specifications

TITLE: Proposal For A Higher Data Rate Frequency Hopping Modulation Scheme

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ABSTRACT

There is a need to select the 'first step up' modulation scheme for higher data rate frequency hopping systems. This is seen as one step in a longer journey where considerably higher data rates are used. In order to make this progression viable, the first step should be taken with a well proven modulation scheme. An equally important factor is implementation, this higher rate must not preclude the use operation of GFSK, and all in a PCMCIA type II form factor. This note shows that $\pi/4$ DQPSK can serve all these needs.

1. INTRODUCTION

One of the great advantages of the proposed modulation scheme is that design and development can start now, there is no need of technology transfer from a single source or the need to prove a modulation scheme. A complete description of $\pi/4$ DQPSK is given. The detail here is sufficient to enable the design and development of systems. It is clearly a modulation scheme that is bandwidth efficient and enables good performance at low cost, hence its selection for the Japanese digital cordless telephone standard.

Ideally with a wireless product, there is freedom for the manufacturer to balance cost versus performance, $\pi/4$ DQPSK has this ability, one can select to develop the 'ideal' system or a lower cost system with very reasonable performance.

The higher data rate inputs have been focused on the use of non linear amplifiers. However this places serious constraints on the data rate achieved or degrades the performance of the radio link. Technically the only route to achieve higher data rates without significant loss of performance is to follow the route of non constant amplitude envelope modulation. One advantage of $\pi/4$ DQPSK is that 'reasonably linear' transmit amplifiers can be used that have acceptable efficiency, not as poor as those assumed to date.

This paper proposes 1.5Mb/sec, not because this is the limit, but because of system implementation issues. This note is a general discussion as to why this modulation scheme should be selected, additional technical information will be presented in Vancouver.

2. MODULATION CHOICE

2.1 Philosophy

The inputs to the choice of modulation scheme are:

- Optimum performance at reasonable cost;
- Proven well defined modulation scheme;
- Flexibility for product developers;
- Compatible with PCMCIA form factor.

Ideally the higher rate modulation scheme (first step up) will offer comparable range performance to the standard 1Mb/sec GFSK. However this should be at reasonable cost. Any modulation scheme selected should be well defined and proven, the market cannot afford the time taken to develop new schemes, the equipment must interwork and in the very near future. As stated earlier, there should be flexibility for lower cost lower performance solutions and higher cost higher performance solutions to enable the manufacturers to target their end market. A final point is that the solution should be compatible with a PCMCIA type II format. This forces the radio to use the same circuits for 1Mb/sec GFSK that are used for the $\pi/4$ DQPSK, as any solution must be dual mode. Now, consider the major decision route as to the modulation scheme selected.

2.2 Orthogonal or Antipodal Modulation Type

There are two basic routes down which the FH group can tread:

- Antipodal type modulation, such as nGFSK, where n denotes the number of levels in the constellation;
- Orthogonal modulation schemes, such as QPSK and nQAM.

Antipodal schemes like nFSK offer the advantage of allowing the use of non linear circuits in transmitter and receiver. However, for each additional bit encoded per symbol there is a 6dB increase in the signal to noise required for a given bit error ratio (BER).

Orthogonal schemes need more linear transmitters and receivers. This technology is not new and can be implemented at reasonable cost. The technical advantage is that only 3dB increase in signal to noise is required for each additional bit encoded per symbol.

So from a baseline 2 level modulation system, the orthogonal modulation for an 8 point constellation will be at least 6dB better than the antipodal system. This equates to 41% to 100% better range depending on the environment. For an infrastructure system providing area coverage this means at least twice the number of access points! Similarly in multipath and interference, the performance difference remains giving the orthogonal schemes an increased range/capacity.

It is proposed that the higher rate FH group adopt the route of orthogonal modulation schemes to enable the best radio range and performance in interference and multipath. The first step is to adopt a variety of QPSK as the four level modulation scheme.

2.3 Implementation Flexibility and Cost Minimisation

To improve the ease of implementation and the robustness of the solution, it is proposed to differentially encode the data (the 'D' in DQPSK). It is acknowledged that this degrades the theoretical coherent Eb/No from 9.5dB to 10.3dB at BER=10^{-5} [1]. All Eb/No figures are quoted at a BER of BER=10^{-5}. This however buys robustness and the ability to use very simple demodulators. A second desire is to use a simple limiter in the receiver, rather than an AGC and to reduce the linearity required in the PA. This is possible by using $\pi/4$ DQPSK, to reduce the peak to mean signal ratio. The performance loss of the limiter is of the order of 1dB, compared to a fully linear coherent system. Again this give the manufacturer the flexibility to trade cost and performance.

A benefit of $\pi/4$ DQPSK is that the existing limiter - discriminator based GFSK receiver circuits can be easily modified to be dual mode. The changes required are in low frequency video analogue and or digital baseband circuits, not in the RF sections.

For a higher degree of circuit integration, digital IF modulators and demodulators using standard CMOS technology, including A/D and D/A conversions can be used. This allow $\pi/4$ DQPSK to be implemented with minimal additional cost over the GFSK receiver. As to whether coherent or non coherent demodulation is used is a matter of choice. A non coherent full Modem, including A/D and D/A conversion circuits takes less than 25k gates on a CMOS circuit. The performance of this circuit is a <14dB Eb/No, including the effect of a 'real' analogue channel filter and a non ideal transmit waveform. For a coherent demodulator, about 10k gates are added and a 2dB improvement is possible in a realistic system. It is a question of choice for the manufacturer which implementation route he selects.

2.4 PA Implementation

One area which may cause concern initially is the PA linearity. However, one should consider the FCC rules and that the control techniques are well understood. In fact this same modulation scheme has been adopted by Japan for their digital cordless standard PHP (Personal Handy Phone). As this is for a consumer, low cost market to compete with analogue cordless phones, it shows that the technical difficulties have been overcome at an affordable cost.

Horror stories of low efficiency of the power amplifiers originate from the need to achieve <-50dBc adjacent channel emissions. For the FCC regulations -20dBc is required.

Additional evidence to proceed down this route is the adoption of QPSK by the DS PHY for 2Mb/sec.

The PA implementation is not a valid argument to preclude the use of orthogonal modulation schemes.

2.5 Data Rate

One of the larger and more expensive circuits on a PCMCIA Type II card WLAN product is the crystal that is used in the reference oscillator. It is only possible to have one per card. Therefore all frequencies generated on the card need to be related to a single reference frequency. This requires all the bit rates to be used to be a logical integer multiples, especially if low cost high performance digital demodulation is used.

Logical steps in data rate are 1, 1.5, 2, 3, e.t.c. It is seen as essential that 1Mb/sec GFSK is supported by the faster mode equipment. With these logical steps there is no technical reason why the two cannot be combined in the same product.

It is proposed that the higher data rates are logically related with simple inter multiples, namely 1, 1.5, 2, 3, 4 ... times the base GFSK data rate.

The proposed modulation scheme is $\pi/4$ DQPSK, with α=0.5. It is possible to achieve 1.6Mb/sec within the FCC rules, but this is not easily related to 1Mb/sec. Therefore the proposed data rate is 1.5Mb/sec for this first step in higher data rates.

DESCRIPTION OF $\pi/4$ DQPSK MODULATION

The modulation proposed $\pi/4$ shifted, differentially encoded quadrature phase shift keying. This uses the phase constellation shown in Figure 1. Note that Gray code is used in the mapping: two di-bit symbols corresponding to adjacent signal phases differ only in a single bit. Note also, the rotation by $\pi/4$ of the basic QPSK constellation for odd (denoted $\oplus$) and even (denoted $\otimes$) symbols.

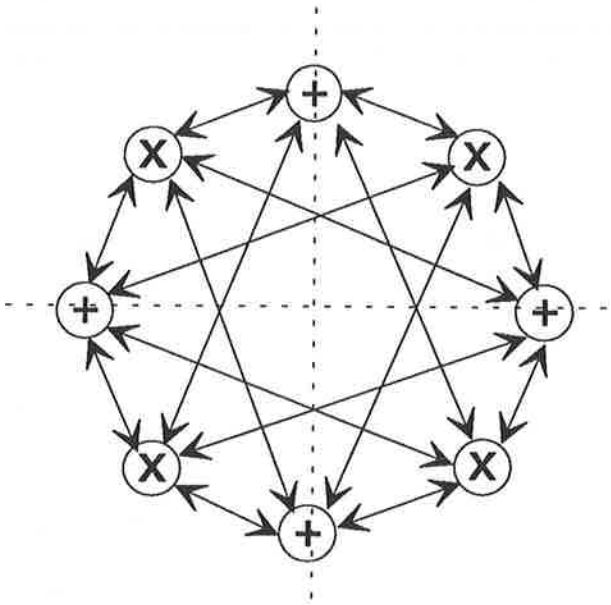

Figure 1.

The information is differentially encoded: symbols are transmitted as changes in phase rather than absolute phases. A block diagram of the differential encoder is shown in Figure 2. The binary data stream entering the modulator, b_m, is converted by a serial-to-parallel converter into two separate binary streams (X_k) and (Y_k). Starting from bit 1 in time of stream b_m, all odd numbered bits form stream X_k and all even numbered bits form stream X_k.

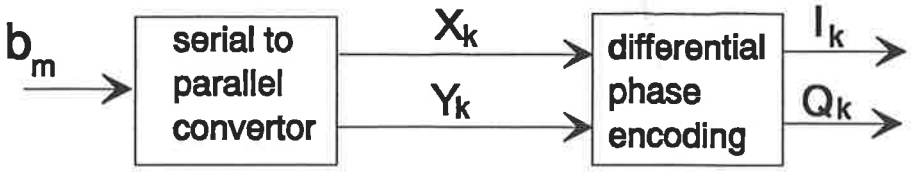

Figure 2

The digital data sequences (X_k) and (Y_k) are encoded onto (I_k) and (Q_k) according to:

$$I_k = I_{k-1} \cos[\Delta\Phi(X_k, Y_k)] - Q_{k-1} \sin[\Delta\Phi(X_k, Y_k)]$$
$$Q_k = I_{k-1} \sin[\Delta\Phi(X_k, Y_k)] + Q_{k-1} \cos[\Delta\Phi(X_k, Y_k)]$$

where I_{k-1}, Q_{k-1} are the amplitudes at the previous pulse time. The phase change $\Delta\Phi$ is determined according to the following table:

X_k	Y_k	$\Delta\Phi$
1	1	$-3\pi/4$
0	1	$3\pi/4$
0	0	$\pi/4$
1	0	$-\pi/4$

The signals I_k,Q_k at the output of the differential phase encoding block can take one of five values 0, ±1, $\pm 1/\pm\sqrt{2}$, resulting in the constellation shown in Figure 1.

Impulses I_k, Q_k are applied to the inputs of the I & Q base-band filters. The base-band filters shall have linear phase and square root raised cosine frequency response of the form:

$$|H(f)| = \begin{cases} 1 & 0 \le f \le \dfrac{1-\alpha}{2T} \\ \sqrt{\frac{1}{2}\left[1-\sin\dfrac{\pi(2fT-1)}{2\alpha}\right]} & \dfrac{(1-\alpha)}{2T} \le f \le \dfrac{(1+\alpha)}{2T} \\ 0 & f > \dfrac{1+\alpha}{2T} \end{cases}$$

where T is the symbol period. The roll-off factor, α, determines the width of the transition band, and is 0.35.

Figure 3 is for explanatory purposes.

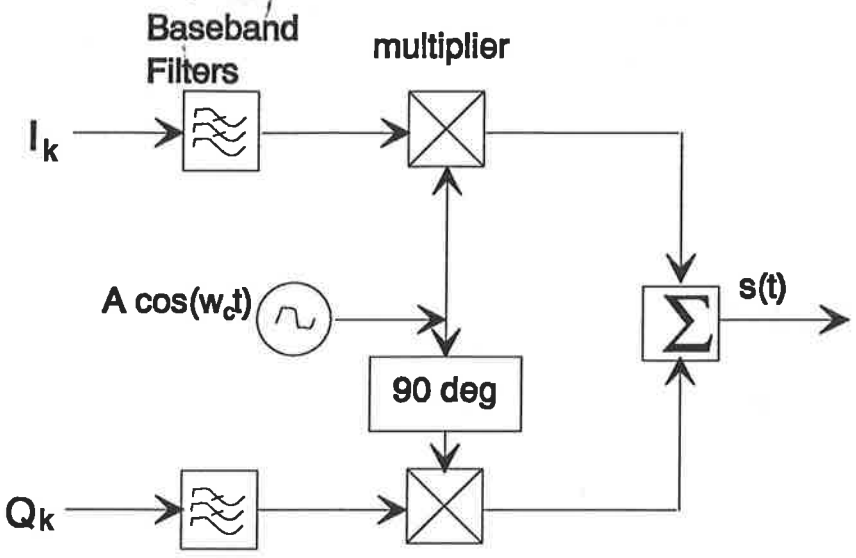

Figure 3

The resultant transmitted signal s(t) is given by:

$$s(t) = \sum_n g(t-nT)\cos\Phi_n \cos\omega_c t - \sum_n g(t-nT)\sin\Phi_n \sin\omega_c t$$

where g(t) is the pulse shaping function ω_c is the radian carrier frequency, T is the symbol period, and Φ_n is the absolute phase corresponding to the n^{th} symbol interval.

The Φ_n which results from the differential encoding is:

$$\Phi_n = \Phi_{n-1} + \Delta\Phi_n.$$

Reference

[1] Proakis J.G, Digital Communications, McGraw Hill, ISBN 0-07-100269-3